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**J.E. (Computer) 1st Semester) EXAMINATION, 2018
COMPUTER ORGANIZATION AND ARCHITECTURE**

(2015 PATTERN)

Two Hours

Maximum Marks : 50

(i) Neat diagrams must be drawn wherever necessary.

(ii) Figures to the right side indicate full marks.

(iii) Use of calculator is allowed.

(iv) Assume suitable data if necessary.

List the elements of Bus Design. Explain any two elements of Bus Design. [6]

Using Booth's algorithm multiplies the following : [6]

Multiplicand = +22

Multiplier = -5

Or

Draw and explain data flow of floating point addition. [6]

Explain Direct cache mapping technique with its advantages and disadvantages. [6]

What are data transfer modes of DMA ? Explain any two in detail. [6]

P.T.O.

(b) Discuss the following I/O mechanisms for transferring data with a neat flowchart : [6]

(i) Programmed I/O

(ii) Interrupt driven I/O

Or

4. (a) What is Machine Instruction ? Explain types of Machine Instructions. [6]

(b) Explain the following addressing modes along with suitable example : [6]

(i) Direct addressing

(ii) Indirect addressing

(iii) Displacement addressing mode

5. (a) Draw and explain the functional block diagram of 8086. [7]

(b) Explain the use of the following registers of 8086 CPU : [6]

(i) General purpose registers

(ii) Segment Register

(iii) Pointer and Index register

(iv) Flag Register

Or

6. (a) Draw and explain instruction cycle state diagram. [7]

(b) Compare superscalar and superpipelined approaches in superscalar processor. [6]

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Explain the following instruction execution phases with suitable example : [7]

- (i) Fetch the instruction
- (ii) Fetch the operand
- (iii) Execute the instruction

Draw and explain Microprogrammed Control Unit. [6]

Or

Explain in detail the following microinstruction sequencing techniques : [6]

- (i) Single Address Fields
- (ii) Variable Address Fields

Name the different design methods for hardwired control units. Explain in detail with any *one* design method. [7]