

No. of Questions—8]

[Total No. of Printed Pages—2

[5459]-193**S.E. (Comp. Engg.) (II Sem.) EXAMINATION, 2018****MICROPROCESSOR****(2015 PATTERN)****2 Hours****Maximum Marks : 50**

- (i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6 and Q. No. 7 or Q. No. 8.
- (ii) Neat diagrams must be drawn wherever necessary.
- (iii) Figures to the right indicate full marks.
- (iv) Assume suitable data, if necessary.

With the help of neat diagram explain how logical address is converted into physical address ? Assume paging mechanism is disabled. [6]

Explain any three control transfer instructions of 80386. [6]

Or

Explain how linear address is converted into physical address by 80386 memory management. [6]

What is the use of the following instructions in 80386 ? Mention which flags gets effected with each instruction : [6]

ADC, DIV, CMP

With the help of suitable diagram, explain how call gate descriptor is used to change the privilege levels, in protected mode ? [6]

Explain the procedure of handling interrupts in protected mode. [6]

P.T.O.

Or

4. (a) What is the role of TSS in multitasking ? Explain I/O permission bitmap in TSS. [6]
- (b) Draw the format of interrupt gate and trap gate descriptor. What is the difference between them ? [6]
5. (a) What is the role of DR0 to DR3 registers in debugging ? Explain task switch breakpoint. [4]
- (b) What are content of CR0 register after RESET in 80386 ? Explain all related bits. [3]
- (c) Explain linear address formation in virtual mode of 80386. [6]
- Or**
6. (a) Explain any four debugging features of 80386. [4]
- (b) List any three differences between Virtual 86 mode and 8086. [3]
- (c) With the help of neat diagram explain format of DR6 register. [6]
7. (a) Compare Pipelined and Non-pipelined bus cycle. [2]
- (b) Explain the following signals of 80386 : MIO#, W/R#, READY# [6]
- (c) Explain the following instructions of 80387 : FLD, FSQRT, FLDZ, FBSTP [5]
- Or**
8. (a) Explain any two instructions used in 80387 to pop data from its stack registers. [2]
- (b) With the help of neat diagram, explain the pipelined read bus cycle. [6]
- (c) When WAIT state is required in 80386 read bus cycle ? Explain with neat diagram. [5]

[5459]-193

2