Total No. of Questions : 8]

SEAT No. :

P3945

[Total No. of Pages : 2

[5462]-668
M.E. (E&TC - VLSI & Embedded System)
ASIC DESIGN
(2017 Course) (Semester - III)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answer any 5 questions.***
2) ***Neat diagrams must be drawn whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Discuss the economics of using ASICs in a product. **[4]**

b) What is ASIC library? What is need of Library? **[4]**

c) What is test bench? **[2]**

Q2) a) What is logic level optimization? **[3]**

b) How full custom ASIC is different from Semi-custom ASIC? **[4]**

c) Explain the different steps in ASIC design flow. **[3]**

Q3) a) Explain timing driven floor planning and placement design flow. **[4]**

b) Explain the final routing steps in ASIC design. **[3]**

c) Discuss different CAD tool features. **[3]**

Q4) a) Which method is most widely used in K L algorithm in system partition steps? **[3]**

b) Explain the concept of Design Reuse. **[2]**

c) Classify the placement algorithms. Explain the min-cut algorithm with the help of example. **[5]**

P.T.O.

Q5) a) What is role of different capacitances in ASIC library design? **[4]**

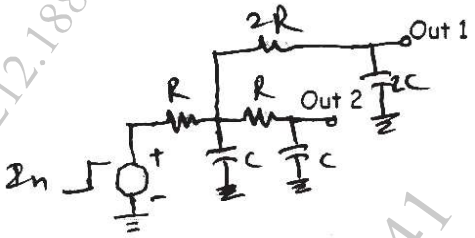
b) Explain different SI issues in ASIC design. **[3]**

b) What are the challenges in Mixed mode design and simulation? **[3]**

Q6) a) Consider the RC network given below : **[5]**

i) Calculate the Elmore's delay from In to Out 1 and from In to Out 2. Which one is critical path?

ii) Assume R = 100Ω and C = 10 pF, Calculate the Elmore's delay of the critical path found in part 1.



b) Explain the concept of pre and post estimation delay in timing analysis? **[3]**

c) What is fault path detection? **[2]**

Q7) a) What is Partial Test? **[2]**

b) Write short note on any 2 : **[4]**

i) JTAG

ii) BILBO

iii) Fault Models

c) What are practical aspects of mix analog digital design? **[4]**

Q8) a) Explain the Synthesis process in detail. **[3]**

b) Explain self test with example. **[3]**

c) What are the different testing approaches for mixed signal Analog and Digital Circuits? **[4]**