

Total No. of Questions : 8]

SEAT No. :

P4376

[Total No. of Pages : 2

[5462]-662

M.E. (E & TC) (VLSI and Embedded Systems)

RECONFIGURABLE COMPUTING

(2017 Pattern)

Time : 3 Hours]

[Max. Marks : 50

Instructions to the candidates:

- 1) Answer any five questions.
- 2) Neat diagram must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Use of Calculator is allowed.
- 5) Assume suitable data if necessary.

- Q1)** a) Explain about flow of program execution for Von Neumann computer architecture. [5]
b) What is mean by instruction level parallelism ,Explain through Example.[5]
- Q2)** a) Explain with diagram single context and multi-context configuration. [4]
b) Explain DSP processor as domain specific processor, give example of DSP processor. [3]
c) Elaborate application of Reconfigurable Computing. [3]
- Q3)** a) With labelled diagram, Explain PAM as Reconfigurable computing platform. [4]
b) Explain partial reconfiguration. w.r.t ASICS. [3]
c) Explain FPGA design flow with necessary diagram. [3]
- Q4)** a) Explain Relocation and Defragmentation w.r.t.RC point of view. [5]
b) Explain Integration of RPF into Traditional Computing Systems. Also explain RaPiD Architecture. [5]
- Q5)** a) With the flow diagram explain FPGA flow design. [5]
b) Explain Non-frequently reconfigurable systems and its application. [5]

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- Q6)** a) Discuss Run time reconfiguration and compile time reconfiguration. [4]
b) Draw diagram and explain the transfer of System from PCB to System on Programmable chip. [4]
c) Write note on FPGA design tools. [2]
- Q7)** a) Explain pattern matching as application of Reconfigurable Computing.[5]
b) How RC is useful for video streaming. [5]
- Q8)** a) Elaborate Reconfigurable Computing for Software Defined Radio. [5]
b) Relate and explain High performance computing and FPGA. [5]

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