Total No. of Questions : 12]

SEAT No. :

P4396

[Total No. of Pages : 3

[5460]-17

T.E. (E & TC) (Semester - II)

COMPUTER ORGANISATION AND ARCHITECTURE

(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two Sections should be written in separate books.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks..***
4) ***Assume suitable data, if necessary.***
5) ***Solve Q.1 or 2, Q.3 or 4, Q.5 or Q.6 from Section I and Q.7 or 8, Q.9 or Q.10, Q.11 or 12 from Section II.***

SECTION - I

Q1) a) Compare Von-Neumann and Harvard architecture. **[6]**

b) Perform (4) × (–5) using Booth's multiplication algorithm. **[12]**

OR

Q2) a) With the help of flow chart explain floating point division operation. **[8]**

b) Describe different IEEE standards for representing floating point numbers. Represent the following in single precision format: **[10]**

i) (10.25)

ii) (–32)

iii) (18)

Q3) a) Draw and explain organization of single bus CPU with control signals. **[8]**

b) What are advantages and disadvantages of Hardwired and micro-programmed control? **[8]**

OR

P.T.O.

Q4) a) Write control sequence of Instruction SUB R3,R1 using single bus organization. **[8]**

b) Using input output gating for the registers in single bus organization explain operation of **[8]**

i) Fetching a word from memory

ii) Storing a word in memory

Q5) a) Write short note on cache memory. **[8]**

b) What are the different methods of handling multiple I/O devices by CPU? **[8]**

OR

Q6) a) Explain interface between keyboard and processor. Also explain communication between them. **[8]**

b) Explain the concept of virtual memory. How virtual address is translated to physical address? **[8]**

SECTION - II

Q7) a) With neat diagram explain the architecture of 8086 processor. **[10]**

b) Explain following instructions: **[8]**

i) MOV AL,[BX]

ii) MOV DL, [1202H]

iii) MOV CX,BX

iv) MOV DL,03H

OR

Q8) a) Explain the minimum and maximum modes of operation in 8086 and pins associated With it. **[10]**

b) Explain any four assembler directives. **[8]**

Q9) a) Explain architecture of 80386 with the help of neat diagram. **[8]**

b) State different types of descriptors and explain in detail segment descriptor. **[8]**

OR

Q10)a) What is paging? How 32 bit physical address is generated in 80386 with paging enabled? **[10]**

b) Explain task switching in 80386. **[6]**

Q11)a) Compare RISC and CISC architectures. **[8]**

b) Explain role of Barrel shifter in ARM core data flow model. **[8]**

OR

Q12)a) Write short note on (any two) : **[8]**

i) Instruction pipelining

ii) Superscalar processor

iii) Tightly couples and loosely coupled Multiprocessor

b) Give classification of various computer architecture for Flynn's classification. **[8]**