Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[4857]-1083

S.E. (I.T.) (First Semester) EXAMINATION, 2015

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right side indicate full marks.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Convert the following numbers, show all steps : [6]

(*i*) $(2598.675)_{10} = (\quad)_{16}$

(*ii*) $(110101.101010)_2 = (\quad)_8$

(*iii*) $(A72E)_{16} = (\quad)_8$

(*b*) Draw and explain CMOS Non-inverting buffer. [6]

Or

2. (*a*) Design full Subtractor using Decoder IC 74138. [6]

(*b*) Explain the following TTL characteristics. [6]

(*i*) Noise Immunity

(*ii*) High level input voltage (V_{IH})

(*iii*) Figure of Merit

P.T.O.

3. (*a*) What is race around condition ? Explain with the help of timing diagram. How is it removed using Flip-flop. [7]

(*b*) Draw and explain 3-bit ring counter. [6]

Or

4. (*a*) Design a sequence generator to generate the sequence .....10110 .....using IC 74194. [7]

(*b*) Design MOD-11 Up counter using IC 74191. [6]

5. (*a*) Design the following functions using PLA. [6]

F1 = Σm (1, 3, 5)

F2 = Σm (5, 6, 7)

(*b*) Draw and explain block diagram of CPLD. [6]

Or

6. (*a*) Explain the difference between CPLD and FPGA. [6]

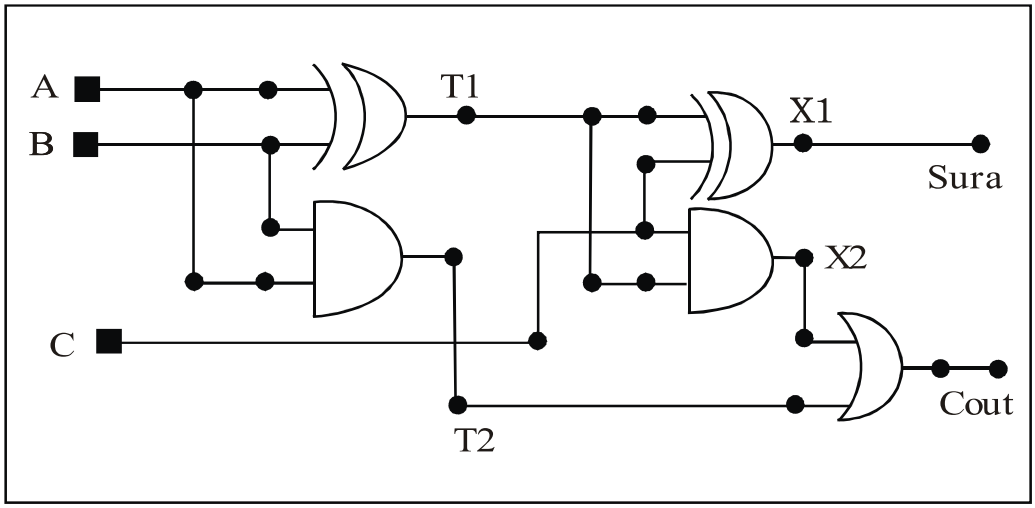
(*b*) Design 4 : 1 Multiplexer using PAL. [6]

7. (*a*) Explain the difference between data flow and behavioural modeling. [7]

(*b*) Write entity and architecture of D Flip-flop with clear input using behavioural modeling. [6]

Or

8. (*a*) Write entity and architecture of following circuit using structural modeling. [7]



(*b*) What is VHDL ? Draw the structure of VHDL module and explain various components of it. [6]