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**[5057]-2062****S.E. (Information Technology) (First Semester)****EXAMINATION, 2016****DIGITAL ELECTRONICS AND LOGIC DESIGN****(2015 PATTERN)****Time : Two Hours****Maximum Marks : 50**

**N.B. :—** (i) Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6 and Q. 7 or Q. 8.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

**1. (a)** Do the following conversions : [6]

(i)  $(27.125)_{10} = (?)_2$

(ii)  $(3A.2F)_{16} = (?)_{10}$

(iii)  $(1101.0011)_2 = (?)_{10}$

(b) How will you connect the output of CMOS logic circuit as an input to TTL logic circuit ? Explain your reason with suitable diagram. [6]

P.T.O.

*Or*

2. (a) Minimize the following function using Quine McClusky and implement using basic logic gates. [6]

$$f(A, B, C, D) = \pi M(1, 2, 3, 8, 9, 10, 11, 14). d(7, 15).$$

- (b) Design full adder using Decoder IC 74138. [6]
3. (a) Explain the difference between asynchronous and synchronous counter and convert SR flip-flop into T flip-flop. Show the design. [6]
- (b) Design and draw logic diagram of Mod 72 counter using IC 7490. [6]

*Or*

4. (a) Draw and explain Johnson counter with initial state 1110 from initial state. Explain all possible states. [6]
- (b) Design sequence generator to generate sequence ..... 1101011..... using shift register IC 74194. [6]
5. (a) What is ASM chart ? Explain MUX controller method using suitable example. [6]
- (b) Implement BCD to Excess-3 code convertor using suitable PLA. [7]

*Or*

- 6.** (a) Implement the following function using PLA : [6]

$$f1 = \Sigma m (0, 3, 4, 7)$$

$$f2 = \Sigma m (1, 2, 5, 7).$$

- (b) Draw the basic structure of CPLD. Explain its feature in brief. [7]

- 7.** (a) What is VHDL ? Explain entity architecture for 2-bit AND and NOR gate. [6]

- (b) Explain the difference between VHDL modeling styles-data flow, behavioral and structural. [7]

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*Or*

- 8.** (a) Write a VHDL code for 4-bit full adder using structural modeling style. [6]

- (b) Explain the following statements used in VHDL with suitable example : [7]

(i) Signal assignment

(ii) Process.