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[5152]-177**S.E. (Information Technology) (Second Semester)****EXAMINATION, 2017****PROCESSOR ARCHITECTURE AND INTERFACING****(2012 PATTERN)****Time : Two Hours****Maximum Marks : 50**

N.B. :— (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,

Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) Explain the following bits of EF lag register in 80386 processor :

(i) IOPL

(ii) VM

(iii) TF. [6]

(b) Explain the assembler directives in 80386 programming :

(i) .model

(ii) .data. [6]

Or

2. (a) Draw the timing diagram of pipelined bus cycle for write operation in 80386. Show status of important signals. [6]

(b) State with examples any six addressing modes of 80386 processor. [6]

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3. (a) Explain with a neat diagram the page translation mechanism in 80386 protected mode. [7]
- (b) What are privileged instructions in 80386 processor ? Explain any *two* privileged instructions. [6]

Or

4. (a) Explain the process of entering and leaving in virtual 8086 mode of 80386. [7]
- (b) Explain with a neat diagram the interrupt Descriptor Table in 80386. [6]

5. (a) Draw and explain the internal memory organization of 8051. [6]
- (b) Draw the functional architecture diagram of 8051 microcontroller. [6]

Or

6. (a) Explain the following instruction of 8051 : [6]
- (i) ADD A, # 10
- (ii) MUL AB
- (iii) MOVC A, @ A + PC
- (b) Compare the following instructions of 8051 : [6]
- (i) RET and RETI
- (ii) SJMP and AJMP.

7. (a) List the interrupts supported by 8051 with their vector addresses & default priorities. [7]
- (b) Explain the TMOD & TCON SFR of 8051 microcontroller. [6]

Or

8. (a) Explain the following SFR of 8051 microcontroller :
- (i) Program Status Word
- (ii) PCON Register. [6]
- (b) Explain Mode 1 and Mode 2 of serial communication in 8051 microcontroller. [7]

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