Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5252]-173

S.E (Information Technology) (I Sem.) EXAMINATION, 2017
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2012 COURSE)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Answer Questions **1** or **2**, **3** or **4**, **5** or **6** and **7** or **8.**
(*ii*) Neat diagrams must be drawn wherever necessary.
(*iii*) Figures to the right indicate full marks.
(*iv*) Assume suitable data, if necessary.

1. (*a*) Explain the following characteristics for TTL logic families :[6]
(*i*) Propagation delay
(*ii*) Figure of merit
(*iii*) Fan In.

(*b*) Design full adder circuit using 4 : 1 Multiplexer. [6]

Or

2. (*a*) Express the following numbers in BCD, Excess-3 and Hexadecimal. Show step by step calculations : [6]
(*i*) $(27)_{10}$
(*ii*) $(396)_{10}$.

(*b*) Design a circuit to find 9's complement of the single digit BCD number using Binary adder IC 7483. [6]

3. (*a*) What is the advantage of MS J-K Flip-Flop ? Explain the working of MS J-K Flip-Flop in detail. [6]

(*b*) Draw and explain the Ring Counter with initial state "10011", from initial state explain all possible states in that Ring.[6]

P.T.O.

Or

4. (*a*) Explain the difference between Combinational and Sequential Circuit. Also convert J-K Flip-Flop to D Flip-Flop. [6]

(*b*) Draw and explain Johnson counter with initial state "1010", from initial state explain all possible states. [6]

5. (*a*) Give the comparison between PROM, PLA and PAL. [6]

(*b*) Design 3-bit Binary to Gray code converter using PLA. [7]

Or

6. (*a*) Explain the difference between CPLD and FPGA. [6]

(*b*) Design the following function using PLA : [7]

F1 = Σm (1, 2, 4, 6) Σ2 = Σm (0, 1, 6, 7) F3 = Σm (2, 6).

7. (*a*) Write a VHDL code for 4 : 1 Mux using Behavioral Modelling. [6]

(*b*) What is VHDL ? What are the important Features of VHDL ? Write Entity and architecture declaration for 2 input AND gate. Assume A and B as input and Z as output of the logic gates. [7]

Or

8. (*a*) What is structural modelling style in VHDL ? Write VHDL code for 2 input EXOR gate with structural modelling. [6]

(*b*) What is the difference between sequential execution and concurrent execution of VHDL statements ? Explain with the help of suitable example. [7]