Total No. of Questions : 6]

SEAT No. :

P1441

[Total No. of Pages : 2

TE/Insem/APR-127
T.E. (Electronics)
FUNDAMENTALS OF HDL
(2015 Pattern)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Ql or Q2, Q3 or Q4, Q5 or Q6.***
2) ***Figures to the right side indicate full marks.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Explore the features of VHDL . **[4]**

b) What do you understand by sequential statement in VHDL? With an example state process statement. **[6]**

OR

Q2) a) With examples, explain different types of scalar data types in VHDL. **[6]**

b) What are the different types of data types in VHDL. **[4]**

Q3) a) Sketch logic block of BCD to 7-seg decoder, write its truth table using common cathode. Write a VHDL program using case statement for common cathode BCD to 7-segment decoder to display from 0 to F. **[6]**

b) What are the different sequential statements in VHDL. **[4]**

OR

Q4) a) Sketch logic block of 8:1 MUX. symbol of MUX and write its truth table. Also sketch its logic gate circuit schematic. **[4]**

b) Describe in brief the use of LIBRARY in Structure of VHDL and also state the values of standard u logic package. **[6]**

P.T.O.

Q5) a) Explain how a 3-variable function is implemented in terms of LUT in FPGA. Given function is F = (a and b) or (not c). **[5]**

b) Sketch the block diagram of CPLD. Describe in brief all the blocks. **[5]**

OR

Q6) a) List down the advantages of FPGA over CPLD. **[5]**

b) Sketch the architecture of FPGA and describe configure logic block in short. **[5]**

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