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[5559]-182

**S.E. (Computer) (First Semester) EXAMINATION, 2019**

**DIGITAL ELECTRONICS AND LOGIC DESIGN**

**(2015 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

*Instructions to the candidates:*

- 1) Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8,
- 2) Neat diagram must be drawn wherever necessary
- 3) Assume suitable data if necessary

Q.1. Solve the following equations using corresponding minimization techniques : [12]

(i)  $Z = f(A, B, C, D) = (2, 7, 8, 10, 11, 13, 15)$

(ii)  $Z = f(A, B, C, D) = (0, 3, 4, 9, 10, 12, 14).$

**OR**

Q.2. a. Solve by Quine-McClusky technique : [8]  
 $Z = f(A, B, C, D) = (0, 1, 3, 4, 6, 8, 10, 12, 14).$

b. Difference between Sequential and Combinational Circuit [4]

Q.3. a. What is an ASM chart ? Give its applications and explain the MUX controlled method with suitable example [6]

b. A combinational circuit is defined by following functions : [6]

$F1 (A,B,C) = \sum m (0,2,4,5), \quad F2 (A,B,C) = \sum m (1,3,6,7)$

Implement this circuit using PLA

P.T.O.

OR

- Q.4. a. What is VHDL ? Explain entity architecture declaration for 2-Bit X-NOR gate [2]
- b. Write VHDL code for 2 bit comparator using data flow Modeling Technique. [5]
- c. Design BCD to Gray code converter and Implement using PLA [5]
- Q.5. a. Draw 2-i/p standard TTL NAND gate with Totem Pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table. [7]
- b. Explain Tristate logic and Tristate TTL inverter [6]

OR

- Q.6. a. Compare CMOS and TTL logic Family [7]
- b. Define the following terms and mention its standard value for TTL logic family. [6]
- 1.Voltage and Current Parameter
  - 2.Power dissipation
  3. Noise Margin
- Q.7. a. State the registers used in Timer counter operation. Explain TMOD register [7]
- b. Draw and explain the Program Status Word of 8051. [6]

OR

- Q.8. a. Explain any three addressing modes of 8051 with example [7]
- b. Explain the function of following pins of 8051 [6]
- i)  $\overline{\text{PSEN}}$
  - ii) RST
  - iii) ALE
  - iv)  $\overline{\text{EA}}$