

Total No. of Questions : 10]

SEAT No. :

P3595

[Total No. of Pages : 3

[5560]-549

T. E. (Electronics)

FUNDAMENTALS OF HDL

(2015 Pattern) (Semester - VI) (End Semester) (304209)

Time : 2½ Hours]

[Max. Marks :70

Instructions to the candidates:

- 1) Answers Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6, Q.7 or Q.8, and Q.9 or Q.10.*
- 2) Neat diagrams must be drawn wherever necessary.*
- 3) Figures to the right indicate full marks.*
- 4) Use of calculator is allowed.*
- 5) Assume suitable data. if necessary.*

Q1) a) What are the different data types of VHDL? with examples explain entity, port and architecture in VHDL. **[6]**

b) What are the different types of descriptions in Verilog HDL? **[4]**

OR

Q2) a) Draw Logic Symbol, truth table and logic gate circuit and write a HDL code for 4:1 MUX using behaviour modeling style by using it statement. **[6]**

b) What is component instantiation in Structural Modeling style of VHDL with an example? **[4]**

Q3) a) State concurrent statements and sequential statements. **[6]**

b) Explain the features of CPLD. **[4]**

OR

Q4) a) Compare SRAM and ANTI - FUSE Technologies used in programming. **[6]**

b) Describe in detail about STD - LOGIC - 1164 library. **[4]**

P.T.O.

- Q5)** a) What is Procedure in Verilog. State its types with example. [8]
 b) What is blocking and non blocking statements in Verilog HDL? [5]
 c) Explain function Syntax with example. [4]

OR

- Q6)** a) Write a Verilog HDL Code for Full Adder using half adder. [8]
 b) What are the differences between continuous and procedural assignments? [9]

- Q7)** a) Write a verilog HDL code for a 4-bit Shift register. [6]
 b) Explain the followig port definitions in Verilog: [6]
 i) Named
 ii) interface
 c) Find the value of following Expressions If the two unsigned variables. [4]

$A = 4'B\ 1011$ and $B = 4'B\ 1101$

- i) $\{A \& \& B\}$
 ii) $(A \parallel B)$
 iii) $\{4\{A\}, 2\{B\}\}$
 iv) $B \gg 2$

OR

- Q8)** a) What are the differences between synchronous and asynchronous finite state machines? [8]
 b) Explain logical and arithmetic operators of verilog Module with examples. [8]
Q9) a) Explain the gate level of abstractions in the Verilog with examples of each. [8]
 b) Briefly explain system tasks in verilog [9]
 i) \$display, \$strobe, \$monitor
 ii) \$time, \$strobe, \$realtime
 iii) \$reset, \$stop, \$finish

OR

Q10) a) Write Verilog HDL code for 4bit - counter [8]

b) Explain the following compiler directives. [5]

i) include Directive with an example

ii) Time Scale with an example

c) Describe the Behavioral description for T Flip-Flop using always Statement. [4]

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