

Total No. of Questions : 6]

SEAT No. :

**P138**

[Total No. of Pages : 1

**OCT/BE/Insem.-63**  
**B.E. (Electronics) (Semester - I)**  
**DSP Processors**  
**(2012 Pattern)**

*Time : 1 Hour]*

*[Max. Marks : 30*

*Instructions to the candidates:*

- 1) *Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.*
- 2) *Neat diagrams must be drawn wherever necessary.*
- 3) *Figures to the right indicate full marks.*
- 4) *Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.*
- 5) *Assume suitable data, if necessary.*

- Q1)** a) Explain decimation and interpolation process using suitable waveforms. [6]  
b) Explain shortly the Analog to Digital conversion errors in context with DSP. [4]

OR

- Q2)** a) What is the difference between DTFT, DFT and FFT. Which is preferred mostly for real time application? Justify. [5]  
b) Write a short note on : Digital Filters. [5]

- Q3)** a) Explain the features to increase the execution speed of the DSP architecture. [6]  
b) List out various data addressing capabilities of DSP architecture? Explain any one briefly. [4]

OR

- Q4)** a) Explain address generation unit used in DSP architecture. [4]  
b) What is Pipelining in DSP architecture? Explain with suitable diagram. [6]

- Q5)** a) Explain the architectural overview of TMS320C54XX DSP processor. [6]  
b) Explain briefly the selection criteria of DSP processors. [4]

OR

- Q6)** a) Explain the architectural overview of TMS320C67XX DSP processor. [6]  
b) Explain shortly various on chip resources available in DSP processor. [4]

