

Total No. of Questions : 6]

SEAT No. :

P131

[Total No. of Pages : 2

OCT/BE/Insem.-56
B.E (Electronics)
VLSI DESIGN
(2012 Pattern) (Semester - I)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Figures to the right side indicate full marks.
- 3) Assume suitable data, if necessary.

Q1) a) Draw pull-up and pull down network. Explain CMOS transistor working in detail. [5]

b) What is channel length modulation and body bias effect. [5]

OR

Q2) a) Derive the expression for power delay product. What is noise margin in CMOS circuit? [5]

b) Implement 4 input Nand gate using CMOS digital logic design. [5]

Q3) a) What do you mean by VHDL? What are the different types of data object? [5]

b) Draw the logic block, truth table and equation of 4:1 MUX and also write a VHDL code for 4 : 1 MUX using dataflow modeling style. [5]

OR

Q4) a) What is function? Explain with suitable VHDL Code. [5]

b) Write a test bench code for a 4 : 1 MUX. [5]

P.T.O.

Q5) a) Draw and explain functional block in CPLD. [5]

b) What are the features of FPGA and CPLD? List down atleast five features. [5]

OR

Q6) a) Explain fast matrix programmable switch in PLD. [5]

b) Compare FPGA with CPLD. [5]

