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Seat No.
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**[5668]-193**

**S.E. (Computer) (II Semester) EXAMINATION, 2019**  
**MICROPROCESSOR AND INTERFACING TECHNIQUES**  
**(2012 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

**N.B. :—** (i) Answer Q. Nos. 1 or 2, 3 or 4, 5 or 6 and 7 or 8.

(ii) Neat diagram must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) Draw and explain block diagram of 8086 microprocessor. [6]  
(b) Explain concept of DOS loadings. [6]

Or

2. (a) Draw and explain block diagram of 8237 DMA controller. [6]  
(b) Draw and explain block diagram of 8259 PIC. [6]

3. (a) Draw and explain block diagram of 8251. [6]  
(b) Explain the functional blocks of 8254 with a neat diagram. [6]

Or

4. (a) Explain different operating modes of PPI 8255. [7]  
(b) Explain different operating modes of DMA controller 8237. [5]

P.T.O.

5. (a) Draw and discuss block schematic of 8484 clock generator and 8286 transceiver. [7]  
(b) Explain internal architecture of 8087. [6]

Or

6. (a) Explain read cycle timing diagram for 8086 minimum mode. [7]  
(b) Explain status and control word of 8087 in detail. [6]

7. (a) Draw block diagram of Intel X58 chipset. [6]  
(b) List features of 8280 JIR I/O controller hub and explain its block components. [7]

Or

8. (a) Draw the block diagram of Intel JCHIO configuration and explain it in detail. [7]  
(b) Explain the following intel @ 82801 IJR I/O controller hub capabilities : [6]

- (i) Direct media interface  
(ii) Serial ATA (SATA) controller.

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