

Seat No.

[5668]-182

**S.E. (Computer Engineering) (I Sem.) EXAMINATION, 2019
DIGITAL ELECTRONICS AND LOGIC DESIGN**

(2015 PATTERN)**Time : Two Hours****Maximum Marks : 50****N.B. :-** (i) Attempt Q. No. 1 or 2, Q. No. 3 or 4, Q. No. 5 or 6,

Q. No. 7 or 8.

(ii) Neat diagram must be drawn wherever necessary.

(iii) Assume suitable data, if necessary.

Q.1. a. Minimize the following logic function using K-map and realize using logic. Draw the diagram for the output [6]

$$F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$$

b. Draw and explain Ring counter using D flip-flop. . Also draw the necessary timing diagram [6]

OR

Q.2. a. Implement the following function using 8:1 MUX and logic gates. [6]

$$F(A, B, C, D) = \sum (0, 2, 5, 8, 10, 15)$$

b. Design 2 bit synchronous UP counter using MS-JK flip flop. Draw the circuit diagram [4]

c. Convert the following flip flop [2]

1. JK to T

Q.3. a. Draw an ASM chart for the 3-bit down counter having one enable line such that: [6]

E=1 (counting enabled)

E=0 (counting disabled) Also draw the state diagram

b. Implement following Boolean function using PAL. [6]

$$F1(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$F2(A, B, C, D) = \sum (2, 12, 13)$$

P.T.O.

OR

Q.4. a. Write VHDL code for 4:1 MUX using dataflow and behavioral modeling [6]

b. Implement the following functions using PLA: [6]

$$F1(A, B, C) = \sum m(1, 2, 4, 6)$$

$$F2(A, B, C) = \sum m(0, 1, 6, 7)$$

Q.5. a. Explain the following characteristics of TTL logic families: [6]

i) Power dissipation. ii) Noise margin. iii) Propagation delay.

b. Draw three input standard TTL NAND gate circuit and explain its operation [7]

OR

Q.6. a. Compare TTL and CMOS logic family [6]

b. Draw and explain the circuit diagram of CMOS inverter [7]

Q.7. a. Describe the classification of instruction set of 8051 with example? [7]

b. Describe the register bank concept in 8051? [6]

OR

Q.8. a. Draw and explain Timer control register (TCON) of microcontroller 8051. [7]

b. Explain the function of following pins of 8051 [6]

i) \overline{EA} ii) $\overline{INT1}$ iii) \overline{PSEN} iv) \overline{RxD}