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Seat No.
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S.E. (Electronics/E&TC) (II Semester) EXAMINATION, 2019

COMPUTER ORGANISATION

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :—

(i) Neat diagrams must be drawn wherever necessary.

(ii) Figures to the right indicate full marks.

(iii) Your answers will be valued as a whole.

(iv) Use of logarithmic tables, slides rule, Mollier charts, electronic pocket calculator and steam tables is allowed.

(v) Assume suitable data, if necessary.

1. (a) What is Bus ? Explain single bus structure in an architecture. [6]

(b) Represent  $(182.1875)_{10}$  in single precision floating point format. [6]

Or

2. (a) Compare RISC and CISC processor. [6]

(b) Explain Booths algorithm with example. [6]

3. (a) Explain with neat diagram single bus organization. [6]

(b) Draw and explain typical DMA block diagram and explain cycle stealing. [6]

P.T.O.

Or

4. (a) Explain the complete control sequence for execution of ADD (R3), R1 Instruction. [6]

(b) Explain daisy chaining method of resolving bus priority in multiprocessor configuration. [6]

5. (a) Compare associative and set-associative mapped cache. [6]

(b) Explain memory hierarchy of Computer System. [7]

Or

6. (a) Write a note on virtual memory. [6]

(b) Explain cache mapping technique. [7]

7. (a) Explain the minimum mode signals and maximum mode signals of 8086. [7]

(b) Explain the function of the following pins of 8086 : [6]

(i) RESET

(ii) M/IO bar

(iii) LOCK.

Or

8. (a) Explain interrupt structure of 8086 processor. [6]

(b) Draw the flag structure of 8086 and explain operation of each flag. [7]

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