

Total No. of Questions : 10]

P2969

SEAT No. :

[Total No. of Pages : 2

[5669]-559

T.E. (Electronics)
FUNDAMENTALS OF HDL
(2015 Pattern)

Time : 2½ Hours]

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Use of calculator is allowed.
- 5) Assume suitable data if necessary.

[Max. Marks : 70

- Q1) a)** What are the different concurrent statements of VHDL? Write a VHDL code by using any one of the concurrent statement for a single bit comparator. [6]
- b)** What are the different types of attributes in VHDL? Give suitable examples. [4]

OR

- Q2) a)** Draw Logic block, symbol, truth table and logic gate circuit of 3:8 Decoder. [4]
- b)** Write a VHDL code using structural modeling style for a full adder by using half adder. [6]

OR

- Q3) a)** Distinguish between Mealy and Moore finite state machines. [6]
- b)** Describe in brief fast switch matrix with a neat sketch. [4]
- Q4) a)** State different technologies used in programming the FPGA. [6]
- b)** Classify HDL operators. [4]

- Q5) a)** Sketch the design flow of ICs in Verilog HDL. [8]
- b)** State different types of system tasks. [5]
- c)** Explain initial and always syntax with example. [4]

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OR

- Q6) a)** Write a Verilog HDL code for 4-bit ALU using case statement. [8]
- b)** Distinguish between task and function. Also list down the similarities of both. [9]

- Q7) a)** What are the different level of abstractions in Verilog HDL state with examples of each. [8]
- b)** What are the reduction operators and represent them by their logic symbol. [4]
- c)** Find the value of following expressions if the two unsigned variables are:
A = 4'B1111 and B = 4'B1001 [4]

- i) {A&&B}
- ii) (A||B)
- iii) {4{A},2{B}}
- iv) B>>2

OR

- Q8) a)** Sketch the logic block, truth table and write a verilog HDL code for a 3-bit up down counter. [8]
- b)** Explain in detail how a task calls a function with an example. [8]

- Q9) a)** Explain shift and rotate logical operators with examples of VHDL and Verilog HDL. [8]
- b)** What are the sequential statements in Verilog HDL. Write a verilog code for a 4:16 decoder using assign statement. [9]

OR

- Q10) a)** What are the data types available in nets for verilog HDL. [8]
- b)** List down the features, compare and contrast of Verilog HDL and VHDL. [9]

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