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[5668]-202

S.E. (I.T.) (Sem. I) EXAMINATION, 2019

**COMPUTER ORGANIZATION AND ARCHITECTURE**

(2015 PATTERN)

**Time : Two Hours****Maximum Marks : 50****N.B. :-** (i) Neat diagrams must be drawn wherever necessary.

(ii) Figures to the right indicate full marks.

(iii) Assume suitable data, if necessary.

1. (a) A benchmark program is run on a 40 MHz processor. The executed program consists of 1,00,000 instruction executions, with the following instruction mix and clock cycle count.

Instruction Type	Instruction Count	Cycles Per Instruction
Integer Arithmetic	45000	1
Data Transfer	32000	2
Floating Point	15000	2
Control Transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program. [6]

- (b) What are addressing modes ? State with example any *three* addressing modes used in the processors. [6]

P.T.O.

Or

2. (a) Using non-restoring algorithm, divide the following unsigned numbers : [6]  
Dividend = 1101  
Divisor = 0011

- (b) Draw and explain instruction cycle state diagram. [6]

3. (a) Explain Hardwired control unit with suitable block diagram. [6]  
(b) A set associative cache consists of 64 lines divided into four line sets. Find various field sizes in memory address. Given that main memory contains 4 K blocks of 128 words each. [7]

Or

4. (a) What is TLB ? Comment on its need and access by processor in address translation process. [6]

- (b) Explain single bus organization of CPU with neat diagram. [7]

5. (a) Explain with suitable block diagram, architecture of MIPS processor. [6]

- (b) What are different types of Hazards in pipelined operation of MIPS ? State their causes. [6]

Or

6. (a) Explain events of Fetch and Execute Cycle. [6]

- (b) Explain code reordering with example to remove data hazards in MIPS pipeline. [6]

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7. (a) What is NUMA ? Draw suitable diagram of NUMA and explain briefly. [6]  
(b) Explain with suitable diagram simultaneous multi-threading. [7]
- Or
8. (a) Draw block diagram of Intel Core i7 organization and explain. [6]  
(b) Write a short note on cluster configuration. [7]