

Total No. of Questions :6]

P33

SEAT No. :

[Total No. of Pages : 1

TE/Insem./APR-37

T.E. (Electronics)

304209 : FUNDAMENTALS OF HDL

(2015 Pattern) (Semester-II)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or 2, Q3 or 4, Q5 or 6.
- 2) Figures to the right indicate full marks.
- 3) Assume suitable data, if necessary.

Q1) a) What do you mean by data types? Explain various data types used in VHDL. [6]

b) What is VHDL? Why it is used . [4]

OR

Q2) a) What is the difference between simulation and synthesis. [4]

b) Explain data flow model and behavioral model with suitable examples. [6]

Q3) a) Write a VHDL code for 1:8 demultiplexer with truth table or excitation table. [6]

b) What is efficient coding styles requirements in VHDL. [4]

OR

Q4) What is the need of PLD? Explain technologies involved it in detail. [10]

a) Discrete technology

b) Application specific integrated CKt

c) PLD technology

Q5) a) Compare CPLD and FPGA. [6]

b) Explain Antifuse programming in FPGA [4]

OR

Q6) a) Explain LOOP statements with two examples. [4]

b) Explain PAL blocks and I/O blocks in CPLD with diagram. [6]

