

Total No. of Questions : 8]

SEAT No. :

P123

[Total No. of Pages : 2

[5871]-628

B.E. (Electronics)

VLSI DESIGN

(2015 Pattern) (Semester - I)

Time : 2 ½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) *Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.*
- 2) *Neat diagrams must be drawn wherever necessary.*
- 3) *Use of logarithmic talbles slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.*
- 4) *Assume suitable data, if necessary.*

Q1) a) Explain CMOS inverter transfer characteristics in detail. What is Bn/Bp ratio? How to achieve this? [8]

b) What is DRC? Explain in detail design rules in CMOS VLSI DESIGN. [8]

c) Write a short note on technology scaling. [4]

OR

Q2) a) Explain in detail static and dynamic power dissipation. what are the components which makes power dissipation in CMOS circuit? [8]

b) Explain the following terms. [8]

i) Body effect

ii) Hot electron effect

iii) Velocity saturation

iv) Power delay product.

c) Write a short note on Transmission gates. [4]

Q3) a) What are different wire parasitics? How do they play important role in routing. [8]

b) Explain clock skew with an example? How to minimize the effect of clock skew? [8]

OR

Q4) a) What are different power distribution techniques available for the VLSI Design. [10]

b) Explain in detail timing consideration. [6]

P.T.O.

Q5) a) Draw the block diagram and explain architecture of CPLD. [8]

b) What is the need of PLD? Explain technologies involved in detail [8]

OR

Q6) a) Explain the difference between logic implemented in CPLD and logic implemented in FPGA. [8]

b) Explain Boundary scan technique. [8]

Q7) a) Explain the need of DFT with suitable examples. [8]

b) Explain fault models in detail. [10]

OR

Q8) Write short note on [18]

i) BIST

ii) JTAG

iii) TAP controller

