Total No. of Questions : 8]

SEAT No. :

P777

[Total No. of Pages : 2

[5870]-1086

T.E. (Electronics)

FUNDAMENTALS OF HDL

(2019 Pattern) (Semester - II)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Figures to the right side indicate full marks.***

Q1) a) Differentiate between CPLD and FPGAS ? **[7]**

b) Describe in brief types of FPGA technologies. **[7]**

c) Explain macrocell with neat diagram. **[6]**

OR

Q2) a) With neat schematic explain the architectural building block of FPGA. **[7]**

b) Explain the following terms related to CPLD **[7]**

i) Functional Blocks / PAL Blocks

ii) I/O Blocks

c) List the basic types of programmable logic Devices. **[6]**

Q3) a) Explain different verilog operators with example in detail. **[8]**

b) Find the value of following expressions if the two unsigned variables A = 4′b 1101 and B = 4′b1001. **[8]**

i) {A & & B} ii) (A || B) iii) {4{A}, 2{B}} iv) B>>2

OR

Q4) a) Write down short notes on following : **[8]**

i) Arrays

ii) Variables & constant declaration

b) Explain verilog modeling styles. **[8]**

P.T.O.

Q5) a) Implement 4 bit synchronous counter using behavioral modeling in verilog HDL. **[8]**

b) Implement 2:4 decoder using dataflow modeling in verilog HDL. **[6]**

c) Write verilog code for half adder in dataflow modeling. **[4]**

OR

Q6) a) Write verilog code for the following flipflops using behavioral modeling in verilog HDL. **[8]**

i) D flip flop

ii) JK flip flop

b) Implement 2:1 multiplexer using case statement in verilog HDL. **[6]**

c) Write verilog code for full adder in dataflow modeling. **[4]**

Q7) a) Explain procedure syntax with example. **[8]**

b) What do you understand by a subprogram? What is subprogram overloading? Explain with VHDL example. **[8]**

OR

Q8) a) Write HDL description of a full adder using Procedure and Task. **[8]**

b) Explain difference between Task and Function. **[8]**

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