Total No. of Questions : 4]

SEAT No. :

P8871

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Oct-22/BE/Insem-77

B.E. (Electronics Engineering)

VLSI DESIGN

(2019 Pattern) (Semester - VII) (404201)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4.***
2) ***Figures to the right side indicate full marks.***
3) ***Assume suitable data, if necessary.***
4) ***Neat diagrams must be drawn wherever necessary.***

Q1) a) Explain about Noise margin in detail. **[3]**

b) Solve the following function using CMOS Digital logic design. **[6]**

i) $F = \overline{A.B+C.D}$

ii) $F = \overline{((A+B+C).D)}$

c) Sketch the Voltage Transfer characteristics of CMOS inverter and explain in detail (include all the regions: Region A, B, C, D, E). **[6]**

OR

Q2) a) Consider an n-channel enhancement-mode MOSFET with the following parameters V_{TN} = 0.4V, W = 20 µm, L = 0.8 µm, μ_n = 650 $cm^2/V–s$, t_{ox} = 100 Å, and ε_{ox} = (3.9) (8.85 × 10^{-14}) F/cm. Find the current when the transistor is biased in the saturation region for V_{GS} = 1.2V. **[3]**

b) Explain in detail : **[6]**

i) Static Power dissipation

ii) Dynamic Power dissipation

c) Explain in detail about the Transmission gates? Sketch the circuit diagram for 2:1 mux using transmission gate. **[6]**

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Q3) a) Compare between VHDL and Verilog. **[3]**

b) Explain different modeling styles (VHDL) used in the design of digital circuits. **[6]**

c) Design and implement VHDL model of one way simple traffic light controller. **[6]**

OR

Q4) a) Compare between Synchronous and Asynchronous Circuits. **[3]**

b) Explain the Test benches in detail. **[6]**

c) Design & implement VHDL model for Melay state machine. **[6]**

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