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|  | WINTER-2023                          |                       |  |
|  | Exam Seat No.:                       |                       |  |
|  | Academic Year:2023-2024              | Semester:I            |  |
|  | Name of Programme:F.Y. M.Tech (E&TC) | Pattern:2022          |  |
|  | Name of Course: ASIC Design          | Course Code:ETC225102 |  |
|  | Max. Marks:60                        | Duration:2.50         |  |

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|  | <p><b>Instructions:</b> Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.</p> <ol style="list-style-type: none"><li>1. This question paper contains 02 page(s).</li><li>2. Answer to each new question is to be started on a new page.</li><li>3. Assume suitable data wherever required, but justify it.</li><li>4. Draw the neat labelled diagrams, wherever necessary.</li><li>5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.</li></ol> |  |
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**Question No. 1 Attempt following Question**

- 1a) Classify ASIC based on Manufacturing. (6) 1

**Question No. 2 Attempt following Question**

- 2a) Explain various types of MOSFET transistor parasitic capacitor (6) 2

**Question No. 3 Attempt following Question**

- 3a) Define Programmable Logic Arrays (PLAs) in ASIC design. How are they utilized in the design process, and what benefits do they offer? (8) 3

**OR**

- 3b) Write VHDL code for 8:1 multiplexer using architecture. (8) 3

- 3c) Difference between VHDL and Verilog (8) 3

**OR**

- 3d) Write short note on EDIF. What role does it play in the design flow ? (8) 3

**Question No. 4 Attempt following Question**

- 4a) Define logic synthesis in the context of ASIC design. Explain the stages involved in logic synthesis and its significance in the design flow. (8) 4

**OR**

4b) Compare the simulation methodologies used in Verilog and VHDL. Mention any significant differences in their simulation processes. (8) 4

4c) Explain the significance of testing in ASIC design. Discuss various testing strategies (8) 4

**OR**

4d) Explain the importance of simulation in the ASIC design process. Discuss the role of Verilog and VHDL simulations in verifying the functionality of a design before synthesis. (8) 4

**Question No. 5 Attempt following Question**

5a) Explain Routing in ASIC design flow (8) 5

**OR**

5b) Identify and discuss the current technological challenges faced in ASIC design (8) 5

5c) Explain floor planning and placement in ASIC design (8) 5

**OR**

5d) Describe the implications of technology scaling on power, performance, and area (PPA) trade-offs in modern ASIC designs. (8) 5