K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

SUMMER-2024	
Exam Seat No.:	
Academic Year:2023-2024	Semester:III
Class:SY	Program:B.Tech
Branch Code:ETC	Pattern:2022
Name of Course:Digital System Design Using HDL	Course Code:ETC222003
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 02 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Question No. 1 Attempt following Question

1a)	Design 1:16 demultiplexer using 1:8 demultiplexer	(6)	CO1

Question No. 2 Attempt following Question

2a)	Design MOD 6 UP counter and explain with the help of waveforms	(6)	CO2

Question No. 3 Attempt following Question

3a)	What is an ASM chart? Give its advantages and applications	(8)	CO3
	OR		
3b)	Design a circuit which follows following sequence 0-3-6-4-1-2-7-0	(8)	CO3
3c)	Design sequence generator to generate the following string of sequence 110011….	(8)	CO3
	OR		
3d)	Compare mealy and Moore machines. What is the lock out condition? And explain how to avoid it.	(8)	CO3

Question No. 4 Attempt following Question

4a)	List and explain data types in VHDL with examples	(8)	CO4
	OR		
4b)	What is an entity and architecture? Write VHDL program for 8:1 multiplexer	(8)	CO4
4c)	With example explain the syntax of while and case statement in VHDL	(8)	CO4

OR

4d)	What are different digital logic families? Give classification of logic families and explain it	(8)	CO4

Question No. 5 Attempt following Question

5a)	Write short notes on VHDL test bench	(8)	CO5

OR

5b)	Write a VHDL program for SR flip flop	(8)	CO5
5c)	Write VHDL code for the 2 bit comparator and also write a test bench for it	(8)	CO5

OR

5d)	Write note on different modeling styles in VHDL along with an example	(8)	CO5

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