



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

SUMMER-2024	
Exam Seat No.:	
Academic Year:2023-2024	Semester:III
Class:SY	Program:B.Tech
Branch Code:INT	Pattern:2022
Name of Course:Digital Electronics and Logic Design	Course Code:INT222004
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains ___3___page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Question No. 1 Attempt following Question

- 1 a) Obtain the Sum of Products (SOP) and Product of Sums (POS) expression using K-map for - (6) CO1
$$Y = f(A,B,C,D) = \sum m (0,4,5,9,11,13,15) + d(2,7)$$

Question No. 2 Attempt following Question

- 2 a) Design a Full Subtractor using K-maps. (6) CO2

Question No. 3 Attempt following Question

- 3 a) Implement $Y_1 = f(A,B,C) = \sum m (0,1,3,7,8,9,12)$ using 8:1 Multiplexer. (5) CO3

OR

- 3 b) Implement Full Adder using 3:8 Decoder. (5) CO3

- 3 c) Implement $Y_1 = f(A,B,C) = \sum m (4,5,7)$ and $Y_2 = f(A,B,C) = \sum m (3,5,7)$ using a Programmable Logic Array. (5) CO3

OR

- 3 d) Implement 8:1 Multiplexer using only 2:1 Multiplexers. (5) CO3

- 3 e) Design an odd parity generator for a 4 bit message. (6) CO3

OR

- 3 f) Write the truth table for a 2 bit comparator and obtain the Boolean expression for the output indicating unequal inputs of the comparator. (6) CO3

Question No. 4 Attempt following Question

- 4 a) Draw and explain the working of clocked S-R Flipflop. (using NAND/NOR Gates) (5) CO4

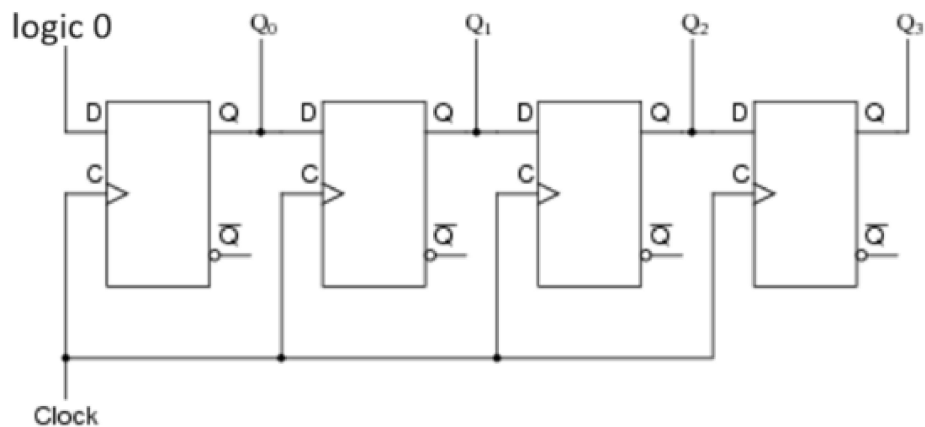
OR

- 4 b) Draw and explain the working of Master Slave J-K Flipflop. (5) CO4

- 4 c) Compare D and T Flipflops. How to obtain D Flipflop from T Flipflop? (5) CO4

OR

- 4 d) Complete the timing diagram for the circuit, assuming all Q outputs begin in the high (logic 1) state. (5) CO4



- 4 e) Obtain the Excitation table of J-K Flipflop. Explain briefly. (6) CO4

OR

- 4 f) Draw and explain 3 bit bidirectional shift register using D Flipflops. (6) CO4

Question No. 5 Attempt following Question

- 5 a) Explain differences between synchronous and asynchronous counters. (4) CO5

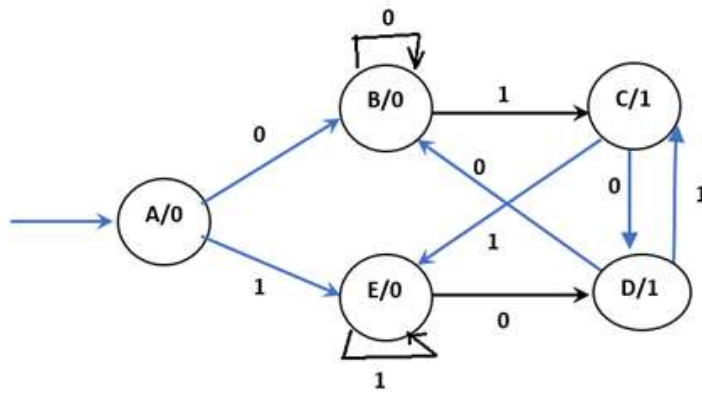
OR

- 5 b) Draw the timing diagram of 3 bit Asynchronous DOWN counter using T Flipflop. Show clock pulse and outputs of all Flipflops. Assume that the Flipflops are with negative edge triggered clock. (4) CO5

- 5 c) Design an Asynchronous MOD-5 counter using 7490. (4) CO5

OR

- 5 d) For the given state diagram, write the state table. (4) CO5



5 e) Design a 3 bit synchronous DOWN Counter using J-K Flipflops.

(8) CO5

OR

5 f) Design a 3 bit sequence detector to detect a sequence 010 arriving on an input X. Use J-K Flipflops.

(8) CO5

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