K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

	InSem Examination-IWinter 2023		
	Exam Seat No.:		
	Academic Year:2023-2024	Semester:I	
	Name of Programme:M.Tech	Pattern:2022	
	Name of Course:ASIC Design	Course Code:ETC225102	
	Max. Marks:30	Duration:1	

	Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use. 1. This question paper contains 2 page(s). 2. Answer to each new question is to be started on a new page. 3. Assume suitable data wherever required, but justify it. 4. Draw the neat labelled diagrams, wherever necessary. 5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question	

Question No. 1 Attempt following Question

a)	Classify ASIC based on Manufacturing.	(7)	1
	OR		
b)	Explain the economics of ASIC	(7)	1
c)	Draw and explain the ASIC design flow	(8)	1
	OR		
d)	Draw the data path structure to build 2 bit adder and the data path symbols for adder	(8)	1

Question No. 2 Attempt following Question

a)	Define and explain logical efforts in detail	(7)	2
	OR		
b)	Explain various types of transistor parasitic capacitor	(7)	2
c)	Draw an explain transistor as switch.	(8)	2

OR

d)	What are optimization target of logic synthesis	(8)	2