



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

	InSem Examination-IWinter 2023		
	Exam Seat No.:		
	Academic Year:2023-2024	Semester:III	
	Name of Programme:B.Tech	Pattern:2022	
	Name of Course:Digital System Design Using HDL	Course Code:ETC222003	
	Max. Marks:30	Duration:1 hr	

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 02 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question

Question No. 1 Attempt following Question

- a) Minimize the following logic function using K-Map and realize using Logic gates (7) CO1

$$F(A,B,C,D)= \Sigma m(0,1,2,3,5,7,9,11,14)$$

OR

- b) Define combinational circuits along with its examples. Implement 16:1 multiplexer using 8:1 multiplexer also write its operation and truth table (7) CO1
- c) Design and implement 2 bit comparator (8) CO1

OR

- d) Design and implement BCD to Excess-3 code converter (8) CO1

Question No. 2 Attempt following Question

- a) Distinguish between synchronous and Asynchronous sequential circuits Write excitation and truth table of T Flip flop (7) CO2

OR

- b) Draw the circuit diagram of SR flip flop and explain its operation with its truth table (7) CO2

- c) Design 2 bit synchronous up counter (8) CO2

OR

- d) Design 4 bit SISO shift register with shift right mode (8) CO2