K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

InSem Examination-IISummer2025	
Exam Seat No.:	
Academic Year:2024-2025	Semester:VI
Class:TY	Program:B.Tech
Branch Code:ETC	Pattern:2022
Name of Course:Advanced Processors	Course Code:ETC223014(C)
Max. Marks:30	Duration:1.15 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 1 page.
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last column indicates the Course Outcome of the Question/sub-question.

		Marks	CO
Question No. 1			
1 a)	Explain Development of the ARM Architecture.	(3)	CO1
1 b)	Explain CMSIS Standard use for Firmware development.	(4)	CO1
Question No. 2			
2 a)	Explain programmer model of ARM CORTEX M4 with neat labelled diagram.	(4)	CO1
2 b)	Differentiate between CORTEX A, R, M processors.	(4)	CO1
	Group OR		
2 c)	Compare initial cortex M family with Cortex M4	(4)	CO1
2 d)	Draw a simple ARM Cortex M4 Architecture diagram.	(4)	CO1
Question No. 3			
3 a)	What is the purpose of the Flash Accelerator in STM32F4xx microcontrollers?	(3)	CO2
3 b)	Draw and explain the memory map of STM32F4XX.	(4)	CO2
Question No. 4			
4 a)	Explain how STM32F4xx supports low-power modes for energy-efficient operation.	(4)	CO2
4 b)	Explain working of DMA in STM32F4xx.	(4)	CO2
	Group OR		
4 c)	Explain key peripherals available in the STM32F4xx series.	(4)	CO2
4 d)	What is the role of the High-Speed External (HSE) and High-Speed Internal oscillator in STM32F4xx? What is role of PLL in Clock generation in STM32F4xx?	(4)	CO2

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