



**K. K. Wagh Institute of Engineering Education & Research, Nashik**  
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2024	
Exam Seat No.:	
Academic Year:2024-2025	Semester:I
Class:PG-I	Program:M.Tech
Branch Code:ETC	Pattern:2024
Name of Course:ASIC Design	Course Code:2402502
Max. Marks:60	Duration:2.30 Hrs.

**Instructions:** Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains two pages.
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

**Marks CO**

**Question No. 1**

- 1a) What is an ASIC cell library? List the types of cells commonly found in an ASIC cell library. (6) CO1

**Question No. 2**

- 2a) Explain the differences between full-custom, semi-custom, and standard cell ASICs? (6) CO2

**Question No. 3**

- 3a) Define low-level design languages. List the key differences between VHDL and Verilog. (8) CO3

**OR**

- 3b) Create a VHDL code for a 4-to-1 multiplexer, including the entity and architecture. (8) CO3
- 3c) Explain the difference between structural modelling and behavioural modelling techniques in VHDL. (8) CO3

**OR**

- 3d) How would you use a schematic entry tool to create a basic logic circuit? (8) CO3

**Question No. 4**

- 4a) Explain how the stuck-at fault model is used to test digital circuits. (8) CO4

**OR**

- 4b) What is a test bench, and why is it important in simulation? (8) CO4
- 4c) Explain the different types of simulation used in ASIC design, from high-level to low-level simulations. (8) CO4

**OR**

- 4d) Define the term "test vector" in the context of ASIC testing. What are the advantages of Boundary-Scan Test in ASIC designs? (8) CO4

**Question No. 5**

- 5a) What is floor planning in ASIC design? Define the term "placement" in the context of integrated circuit design. (8) CO5

**OR**

- 5b) What are some common techniques for reducing power consumption in ASIC design? (8) CO5
- 5c) What is routing in the context of ASIC design? List two common routing algorithms used in integrated circuit design. (8) CO5

**OR**

- 5d) **Explain** the difference between static and dynamic power consumption in VLSI designs. (8) CO5

..... **End of question paper**.....