

Question No. 1

- 1a) How many delay models are there? Explain any one in detail. (6) CO1

Question No. 2

- 2a) What is fault dominance in fault testing, and how does it simplify the testing process? (6) co2

Question No. 3

- 3a) What are the key principles of self-checking design? (8) CO3

OR

- 3b) Explain the concept of redundancy in self checking system and its role in detecting faults. (8) CO3

- 3c) What is a self-checking checker, and how does it differ from a regular checker? (8) CO3

OR

- 3d) A system has a 7-bit output with a self-checking design. How many errors can the system detect if it uses a single parity bit (8) CO3

Question No. 4

- 4a) Explain BIST and its testing levels (8) CO4

OR

- 4b) Explain in brief Scan and boundary scan architecture (8) CO4

- 4c) Describe the JTAG standard and its role in modern digital testing (8) CO4

OR

- 4d) What are the different states of the JTAG state machine, and how do they support testing (8) CO4

Question No. 5

- 5a) What is (DFT) in embedded core systems? (8) CO5

OR

- 5b) What is hardware emulation and how does it differ from simulation? Give its example. (8) CO5

- 5c) What is model checking and how is it used in formal verification? (8) CO5

OR

- 5d) What are the limitations of formal verification techniques? How does formal verification ensure the correctness of a design. (8) CO5

..... **End of question paper**.....