K. K. Wagh Institute of Engineering Education & Research, Nashik

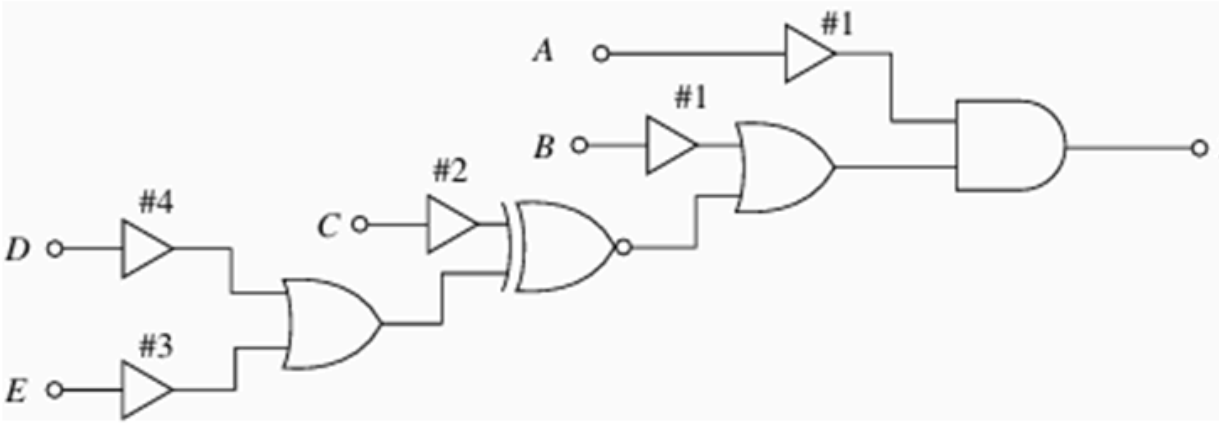
(An Autonomous Institute From A.Y. 2022-23)

InSem Examination-I Winter2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:I
Class:PG-I	Program:M.Tech
Branch Code:ETC	Pattern:2024
Name of Course: VLSI Design Verification and Testing	Course Code:2402503
Max. Marks:30	Duration:1.15 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 1 page.
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

		Marks	**CO**
Question No. 1			
1 a)	Define and explain hazard detection in combinational logic circuits. Describe static and dynamic hazards and methods to Eliminate them.	(7)	CO1
Question No. 2			
2 a)	Discuss different types of simulation used in VLSI verification.Compare interpreted, compiled, and event-driven simulations with respect to speed and accuracy.	(8)	CO1
	OR		
2 b)	Assume that the buffers in Figure have delays indicated by the numbers following the pound signs, and assume that all gates have zero delay. Also assume a signal change from A,B,C,D,E = (0,1,1,1,0) to A,B,C,D,E = (1,0,0,0,1) occurs. How many evaluations are required by an event-driven simulator to determine the state of the circuit?	(8)	CO1



Question No. 3

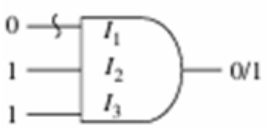
3 a) Describe fault detection and redundancy in digital circuits.How does redundancy affect testability and circuit reliability? (7) CO2

Question No. 4

4 a) Explain the single stuck-at fault model. Discuss how single stuck-at faults are detected using test vectors . (8) CO2

OR

4 b) Create the truth table for a three-input OR gate corresponding to that of the AND gate in Figure Show the response for SA0 faults on the inputs and the SA0 and SA1 faults on the output. (8) CO2



	I_1	I_2	I_3	G	F_1	F_2	F_3	F_4	F_5
$F_1 - I_1$ SA1	0	0	0	0	0	0	0	0	1
$F_2 - I_2$ SA1	0	0	1	0	0	0	0	0	1
$F_3 - I_3$ SA1	0	1	0	0	0	0	0	0	1
$F_4 - Out$ SA0	0	1	1	0	1	0	0	0	1
$F_5 - Out$ SA1	1	0	0	0	0	0	0	0	1
	1	0	1	0	0	1	0	0	1
	1	1	0	0	0	0	1	0	1
	1	1	1	1	1	1	1	0	1

····· End of question paper·····