



**Marking Scheme SET 1  
End-Sem Examination-I, Winter 2025**

Academic Year: 2025-2026	Semester: I
Class: FYMTECH	Program: PG In VLSI & Embedded System
Branch Code: ETC	Pattern: 2024
Name of Course: Embedded Product Design	Course Code: 2402501

<b>Q. No.</b>	<b>Details</b>	<b>Max. Marks</b>
Q.1.	Need (3 Marks): Role in daily life, automation, real-time control, IoT. Challenges (3 Marks): Any four of: Balancing Performance/Power/Cost, Complex Software Stacks, Tight H/W-S/W Integration, Real-Time Constraints, Security, Debugging complexity.	[6]
Q.2.	Features of V-Model (4 Marks): Explanation of the V-shape, parallel verification (left side) and validation (right side), clear traceability, early detection of defects. Suitability (2 Marks): Emphasis on systematic approach, rigorous testing at each stage, alignment with functional safety standards (e.g., ISO 26262), enhancing reliability.	[6]
Q.3.	a) GPP vs. Custom Processor Trade-offs (8 Marks): Comparison table/points focusing on: Time-to-Market (GPP is faster), Energy Efficiency (Custom is better), Flexibility (GPP is higher), NRE Cost (Custom is higher).  OR  b) Firmware Role & Stages (8 Marks): Role (3M): Low-level interaction, controls hardware, ensures reliability. Stages (5M): Bootloader execution, Hardware initialization (peripherals, clock), RTOS/OS loading (if applicable), Application thread/task execution.  c) Interfacing & ADC Functional Blocks (8 Marks): Interfacing Definition (2M). Functional Blocks (6M): Sensor, Signal Conditioning (Amplification/Filtering), ADC Chip, Control Logic (Start Conversion, EOC monitoring), Data Bus/Interface (SPI/I2C), Microcontroller. Diagram is optional but adds value.  OR  d) FPGA Design & Selection vs. ASIC (8 Marks): FPGA use (4M): Prototyping, low/medium volume, parallel processing, faster time-to-market, reprogrammability. Selection criteria vs. ASIC (4M): Preferred when NRE is high, volume is low, or requirements change frequently.	[8]  [8]  [8]



