



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:I
Class:PG-I	Program:M.Tech
Branch Code:ETC	Pattern:2024
Name of Course:ASIC Design	Course Code:2402502
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Marks CO

Question No. 1

- 1a) Explain the essential contents and purpose of an ASIC standard cell library. Why are cells pre-characterized for attributes like timing and power? (6) CO1

Question No. 2

- 2a) Explain the concept of a "half-gate" or minimal/segmented logic block as used in some programmable ASIC architectures. (6) CO2

Question No. 3

- 3a) Compare between behavioral modeling and RTL modeling in VHDL or Verilog. (8) CO3

OR

- 3b) Explain the importance of the Electronic Design Interchange Format (EDIF) in a multi-vendor ASIC toolchain. (8) CO3

- 3c) Describe the current role of schematic entry in a modern, complex ASIC design flow. (8) CO3

OR

- 3d) What is the primary optimization goal of a PLA tool? Explain how techniques like logic minimization (e.g., Quine-McCluskey or Espresso) are used to reduce the size and complexity of the resulting PLA implementation. (8) CO3

Question No. 4

- 4a) Explain the three major phases of the Logic Synthesis process: Translation/Elaboration, Optimization, and Technology Mapping. (8) CO4

OR

- 4b) Define and distinguish between Code Coverage (line, branch, condition) and Functional Coverage (using System Verilog as an example). (8) CO4

- 4c) Explain the concept of Design for Testability (DFT), focusing on the common technique of Scan Chain Insertion. (8) CO4

OR

- 4d) Explain the concept of synthesizable RTL code in VHDL/Verilog. (8) CO4

Question No. 5

- 5a) Explain the primary goals of Floor Planning (Meeting die size, minimizing wire length, creating power distribution). (8) CO5

OR

- 5b) Why is the Routing stage critical for final design closure? Explain in detail. (8) CO5

- 5c) Differentiate between the Global Routing and Detailed Routing phases. (8) CO5

OR

- 5d) What is the core objective of the Placement stage, following floor planning? (8) CO5

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