# K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

| WINTER-2025 | |
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| Exam Seat No.: | |
| Academic Year:2025-2026 | Semester:I |
| Class:PG-I | Program:M.Tech |
| Branch Code:ETC | Pattern:2024 |
| Name of Course:VLSI Design Verification and Testing | Course Code:2402503 |
| Max. Marks:60 | Duration:2.30 Hrs. |

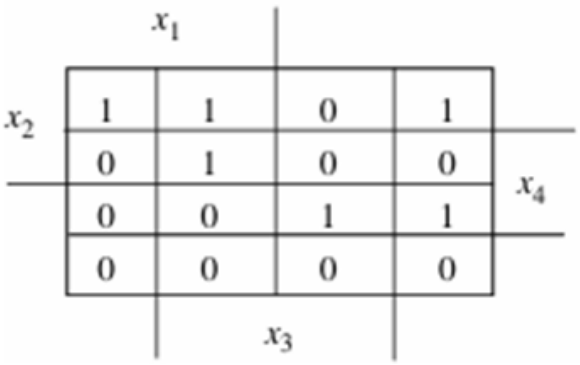
**Instructions:** Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

**Marks CO**

**Question No. 1**

1a) For the Karnaugh map in Figure. (6) CO1




(a) Identify a 1-hazard.

(b) Identify all transitions for which 1-hazards can be avoided.

(c) Find a dynamic hazard

Question No. 2

2a) Describe fault detection and redundancy in digital circuits. How does redundancy affect testability and circuit reliability? (6) CO2

Question No. 3

3a) Explain the difference between lossy and lossless compression techniques. (8) CO3

OR

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|---|---|---|---|
| 3b) | Difference between self-checking checker and regular checker? | (8) | CO3 |
| 3c) | What is the parity-check function, and how is it applied in error detection? | (8) | CO3 |

OR

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|---|---|---|---|
| 3d) | How does a totally self-checking equality checker help in fault detection? Explain it with Example. | (8) | CO3 |

Question No. 4

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|---|---|---|---|
| 4a) | What is the principle of scan and boundary scan architecture. Explain it with any example. | (8) | CO4 |

OR

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|---|---|---|---|
| 4b) | How does the Linear Feedback Shift Register (LFSR) generate test patterns? Why is BIST considered essential for testing at the chip level? | (8) | CO4 |
| 4c) | What is an analog test bus, and what role does it play in electronic testing? | (8) | CO4 |

OR

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|---|---|---|---|
| 4d) | Describe the key features of the Joint Test Action Group (JTAG) and how they apply to analog testing? | (8) | CO4 |

Question No. 5

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| 5a) | What is the purpose of timing verification in VLSI design?What are the common tools used for timing verification? | (8) | CO5 |

OR

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|---|---|---|---|
| 5b) | Describe the concept of coverage-driven verification. How do verification techniques improve functional verification? | (8) | CO5 |
| 5c) | How equivalence checking is important in the design verification process? How combinational Checking is different from sequential equivalence checking. | (8) | CO5 |

OR

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|---|---|---|---|
| 5d) | Difference between formal verification and smulation based verification. | (8) | CO5 |

**····· End of question paper·····**