



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:I
Class:PG-I	Program:M.Tech
Branch Code:ETC	Pattern:2024
Name of Course:Static Timing Analysis	Course Code:2402504(B)
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Marks CO

Question No. 1

- 1a) Explain the differences between functional verification and timing verification. (6) CO1

Question No. 2

- 2a) Discuss the factors that influence the propagation delay in CMOS circuits. (6) CO2

Question No. 3

- 3a) Explain the Linear Timing Model (LTM) used in digital circuit timing analysis. (8) CO3

OR

- 3b) With neat diagrams, explain the timing arcs present in a combinational logic cell. (8) CO3

- 3c) A logic gate shows a delay of 0.20 ns using a linear timing model for a load of 20 fF. However, NLDM characterization gives a delay of 0.28 ns for the same load and input transition. Calculate the percentage error introduced by the linear timing model and explain the reason for this difference. (8) CO3

OR

- 3d) Compare Linear Timing Models and Non-Linear Delay Models. (8) CO3

Question No. 4

- 4a) Explain the **RLC model of on-chip interconnects**. (8) CO4

OR

- 4b) Explain the need for wire load models during the **pre-layout phase** of VLSI design. (8) CO4

- 4c) A metal interconnect line of length 2 mm has a resistance of $0.08 \Omega/\mu\text{m}$ and capacitance of $0.25 \text{ fF}/\mu\text{m}$. The line is driven by a gate with output resistance 120Ω and drives a load capacitance of 30 fF. Calculate the interconnect delay using the Elmore delay model. (8) CO4

OR

- 4d) Explain various techniques used to **reduce parasitic resistance and capacitance** in critical nets. (8) CO4

Question No. 5

- 5a) What are **generated clocks** in STA? Explain how they are created from master clocks and discuss their importance in analyzing divided, multiplied, and gated clock paths. (8) CO5

OR

- 5b) What is **path segmentation in STA**? Explain how timing paths are segmented into clock path, data path, and capture path, and discuss its benefits in accurate timing analysis (8) CO5

- 5c) Explain the techniques used to **refine timing analysis** in STA. Discuss the impact of clock uncertainty, on-chip variation (OCV), advanced OCV (AOCV), and pessimism reduction techniques. (8) CO5

OR

- 5d) Define **timing path groups** in STA. Explain how paths are categorized (register-to-register, input-to-register, register-to-output, input-to-output) and their role in timing optimization. (8) CO5

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