K. K. Wagh Institute of Engineering Education and Research, Nashik

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Academic Year: 2025-2026 | **Semester: I**

Name of Programme: M.Tech | **Pattern: 2024**

Name of Course: Static Timming Analysis | **Course Code: 2402504(B)**

Max. Marks: 60* | **Duration: 2:30 Hr.**

<table>
<tr><th>Q. No.</th><th>Details</th><th>Max. Marks</th><th>CO No.</th><th>BT Level</th></tr>
<tr><td>Q.1</td><td>Explain the differences between functional verification and timing verification.

Ans:
<table><tr><th>Aspect</th><th>Functional Verification</th><th>Timing Verification</th></tr><tr><td>Purpose</td><td>Checks whether the circuit performs the intended logic function</td><td>Checks whether signals meet required timing constraints</td></tr><tr><td>What is verified</td><td>Logical correctness of design</td><td>Setup time, hold time, and path delays</td></tr><tr><td>Consideration of time</td><td>Logical behavior, often ignores real delays</td><td>Explicitly considers delays and clock constraints</td></tr><tr><td>Method used</td><td>Simulation using test vectors</td><td>Static Timing Analysis (STA) or timing simulation</td></tr><tr><td>Input dependency</td><td>Requires functional test vectors</td><td>Vectorless (in STA)</td></tr><tr><td>Stage of use</td><td>Early and throughout design flow</td><td>Mainly after synthesis and layout</td></tr></table></td><td>[6]</td><td>CO1</td><td>L2</td></tr>
<tr><td>Q.2</td><td>Discuss the factors that influence the propagation delay in CMOS circuits.

Ans:
• Load Capacitance
Higher output capacitance increases charging/discharging time, leading to larger delay.
• Input Transition Time (Slew)
Slow input transitions reduce the effective drive strength of transistors, increasing delay.</td><td>[6]</td><td>CO2</td><td>L2</td></tr>
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	• **Transistor Sizes (W/L ratio)** Larger transistors have lower resistance and hence smaller delay. • **Supply Voltage (VDD)** Lower VDD reduces drive current, increasing propagation delay. • **Process, Voltage, and Temperature (PVT) Variations** Variations in fabrication and operating conditions affect delay significantly. • **Interconnect Resistance and Capacitance** Long wires add parasitic R and C, increasing overall path delay.			
Q.3	a) Explain the Linear Timing Model (LTM) used in digital circuit timing analysis. Ans: The **Linear Timing Model (LTM)** is a simplified delay model used in early digital timing analysis where gate delay is assumed to vary linearly with output load. **Explanation:** • In LTM, the propagation delay of a logic gate is expressed as: $t_{pd} = t_0 + k \cdot C_L$ where t_0= intrinsic delay of the gate k= delay sensitivity constant C_L= output load capacitance • The model assumes: o Constant input transition time o Linear dependence of delay on load o Negligible non-linear effects **Characteristics:** • Easy to compute and implement • Useful in **pre-layout** or early design stages • Does not consider input slew variation **Limitations:** • Inaccurate for deep submicron designs • Ignores non-linear transistor behavior **OR**	[16]	CO3	L3

b) With neat diagrams, explain the timing arcs present in a combinational logic cell.

Ans:

Timing Arcs:

A **timing arc** represents the delay relationship between an input pin and an output pin of a logic cell.

Types of Timing Arcs:

1. **Rising Input → Rising Output (pos_unate)**
2. **Falling Input → Falling Output (pos_unate)**
3. **Rising Input → Falling Output (neg_unate)**
4. **Falling Input → Rising Output (neg_unate)**

Explanation:

- **Positive unate:** Output transitions in the same direction as input (e.g., buffer).
- **Negative unate:** Output transitions in opposite direction (e.g., inverter).
- **Non-unate:** Output transition depends on logic state of other inputs (e.g., NAND, NOR).

Importance:

- Used in STA to calculate delay and slew
- Stored in standard cell libraries

c) A logic gate shows a delay of 0.20 ns using a linear timing model for a load of 20 fF. However, NLDM characterization gives a delay of 0.28 ns for the same load and input transition. Calculate the percentage error introduced by the linear timing model and explain the reason for this difference.

Ans:

Given:

- LTM delay = 0.20 ns
- NLDM delay = 0.28 ns

Percentage Error Calculation:

$$\text{Error} = \frac{0.28 - 0.20}{0.28} \times 100$$

$$= \frac{0.08}{0.28} \times 100 = 28.57\%$$

CO3 L3

OR

d) Compare Linear Timing Models and Non-Linear Delay Models.

Ans:

Aspect	LTM	NLDM
Delay relation	Linear	Non-linear
Input slew	Ignored	Considered
Accuracy	Low	High
Load modeling	Approximate	Accurate
Usage	Early design	Modern STA
Technology suitability	Older nodes	Deep submicron
Library format	Equation-based	LUT-based
Industry usage	Rare	Standard

Q.4

a) Explain the **RLC model of on-chip interconnects**.

Ans:

The **RLC model** represents interconnects using:

- **R** – Resistance (due to metal lines)
- **L** – Inductance (due to current flow)
- **C** – Capacitance (to substrate and neighbors)

Importance:

- Resistance causes delay and IR drop
- Capacitance slows signal transitions
- Inductance causes ringing and overshoot

Applicability:

- Important for **long global interconnects**
- High-speed and clock networks

OR

b) Explain the need for wire load models during the **pre-layout phase** of VLSI design. [16] CO4 L2

Ans:

Need for Wire Load Models:

- Routing is unknown during pre-layout
- Exact parasitics are unavailable

Purpose:

- Estimate interconnect capacitance
- Predict delay for synthesis and STA
- Enable early timing closure

Limitations:

- Based on statistical averages
- Inaccurate for deep submicron nodes

c) A metal interconnect line of length 2 mm has a resistance of 0.08 Ω/μm and capacitance of 0.25 fF/μm. The line is driven CO4 L3

	by a gate with output resistance 120 Ω and drives a load capacitance of 30 fF. Calculate the interconnect delay using the Elmore delay model. Ans: • Length = 2 mm = 2000 µm • Resistance = 0.08 Ω/µm → Total R = 160 Ω • Capacitance = 0.25 fF/µm → Total C = 500 fF • Driver resistance = 120 Ω • Load capacitance = 30 fF **Elmore Delay:** $t_d = R_d(C_{wire} + C_L) + \frac{1}{2}R_{wire}C_{wire}$ $= 120(500 + 30)fF + \frac{1}{2}(160)(500fF)$ $= 63.6ps + 40ps = 103.6ps$ **OR** d) Explain various techniques used to **reduce parasitic resistance and capacitance** in critical nets. Ans: • Use wider metal lines • Use higher metal layers • Shorten interconnect length • Shield critical nets • Insert repeaters • Optimize routing topology • Reduce coupling capacitance • Use low-k dielectrics			
Q.5	a) What are **generated clocks** in STA? Explain how they are created from master clocks and discuss their importance in analyzing divided, multiplied, and gated clock paths. Ans: Generated clocks are derived from master clocks using: • Frequency dividers • Multipliers (PLL)	[16]	CO5	L2

	• Gating logic They are defined using **create_generated_clock**. **Importance:** • Accurate analysis of derived clock domains • Prevents false timing violations **OR** b) What is **path segmentation in STA**? Explain how timing paths are segmented into clock path, data path, and capture path, and discuss its benefits in accurate timing analysis. Ans: **Path segmentation in Static Timing Analysis (STA)** is the systematic division of a complete timing path into logical sections so that timing delays, uncertainties, and constraints can be analyzed accurately and independently. Instead of treating the timing path as a single monolithic delay, STA breaks it into **clock-related and data-related segments**, allowing precise modeling of real silicon behavior. In synchronous digital circuits, a timing path is typically segmented into: 1. **Clock Launch Path** 2. **Data Path** 3. **Clock Capture Path** This segmentation is fundamental to reliable **setup and hold timing analysis**.			
	c) Explain the techniques used to **refine timing analysis** in STA. Discuss the impact of clock uncertainty, on-chip variation (OCV), advanced OCV (AOCV), and pessimism reduction techniques. Ans:		CO5	L2

1. Clock uncertainty represents the possible variation in clock arrival times due to:

- Clock jitter (short-term variations)
- Clock skew (differences in arrival time)
- Modeling inaccuracies

Impact on Timing:

- Reduces the available time for data propagation
- Tightens setup and hold timing margins
- Included as a margin in STA to prevent timing failures

2. On-Chip Variation (OCV)

On-Chip Variation (OCV) accounts for process, voltage, and temperature (PVT) variations **within a single chip**.

Key Features:

- Different parts of the chip may experience different delays
- Applies derating factors to cell and interconnect delays

Impact on Timing:

- Increases delay uncertainty
- Often leads to pessimistic timing results

3. Advanced On-Chip Variation (AOCV)

Advanced OCV (AOCV) is an enhancement over traditional OCV that provides **path-depth dependent derating**.

Key Features:

- Derating depends on the number of stages (logic depth)
- Uses lookup tables based on path length and cell type

	• More realistic than fixed OCV derates **Impact on Timing:** • Reduces unnecessary pessimism • Improves correlation between STA and silicon performance **4. Pessimism Reduction Techniques** **a) Common Path Pessimism Removal (CPPR)** • Removes double-counting of variations on shared clock paths • Applied when launch and capture clocks share common segments **b) Clock Reconvergence Pessimism Removal** • Eliminates excessive skew assumed after clock reconvergence **Impact:** • Improves achievable slack • Reduces false timing violations **OR** d) Define **timing path groups** in STA. Explain how paths are categorized (register-to-register, input-to-register, register-to-output, input-to-output) and their role in timing optimization. Ans: **1. Register-to-Register (Reg → Reg) Paths** **Definition:** Paths that start at the output of a launching flip-flop and end at the input of a capturing flip-flop. **Characteristics:** • Most common and critical path group			

- Controlled by the same or related clocks
- Subject to **setup and hold time constraints**

Role in Timing Optimization:

- Primary focus during timing closure
- Optimized using logic restructuring, gate sizing, buffering, and clock skew management
- Determines the **maximum operating frequency** of the design

2. Input-to-Register (In → Reg) Paths

Definition:
Paths that start at a **primary input port** and end at a register inside the chip.

Characteristics:

- Data is launched by an external device
- Requires **input delay constraints** to model external timing

Role in Timing Optimization:

- Ensures compatibility with external interfaces
- Optimized by adjusting input delay constraints, I/O buffering, and input timing budgets
- Prevents setup and hold violations at the first register stage

3. Register-to-Output (Reg → Out) Paths

Definition:
Paths that start at an internal register and end at a **primary output port**.

Characteristics:

- Data is captured by an external device

- Requires **output delay constraints**

Role in Timing Optimization:

- Ensures correct data delivery to external systems
- Optimization involves output buffering, drive strength tuning, and timing budget allocation
- Important for meeting interface timing specifications

4. Input-to-Output (In → Out) Paths

Definition:
Purely combinational paths that start at a primary input and end at a primary output without passing through registers.

Characteristics:

- Often represent combinational logic blocks
- May not be clocked paths

Role in Timing Optimization:

- Checked against maximum delay constraints
- Often declared as **false paths** if not functionally active
- Optimized by logic simplification or constrained explicitly

Role of Timing Path Groups in Timing Optimization

1. **Focused Timing Closure**
   Allows designers to prioritize critical path types (e.g., Reg → Reg) without over-constraining others.
2. **Independent Constraint Handling**
   Different constraints (clock, input delay, output delay) can be applied accurately.
3. **Efficient Debugging**
   Helps isolate timing violations to specific path types.

	4. **Performance Optimization** Enables selective optimization to improve slack where it matters most. 5. **Reduction of Over-Constraint** Prevents unnecessary pessimism by separating unrelated timing paths.			