K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:VII
Class:FINAL	Program:B.Tech
Branch Code:ETC	Pattern:2022
Name of Course:VLSI Testing and Testability	Course Code:ETC224006B
Max. Marks:30	Duration:1.15 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 pages.
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. Question no. 1 and 2 are compulsory.

		Marks	CO
Question No. 1			
1	What is the need for verification in VLSI design?	(3)	CO1
Question No. 2			
2	Write the general form of a March test sequence.	(3)	CO2
Question No. 3			
3.a)	Discuss the role of multiplexers in DFT architecture.	(4)	CO3
	OR		
3.b)	Compare scan chain testing and boundary scan testing.	(4)	CO3
3.c)	How does the analog test bus facilitate mixed-signal testing?	(4)	CO3
	OR		
3.d)	Draw and Explain Wrapper Architecture.	(4)	CO3
Question No. 4			
4.a)	How does formal verification improve design correctness?	(4)	CO4
	OR		
4.b)	Describe the difference between soft, firm, and hard cores in testing.	(4)	CO4
4.c)	What are the advantages of using hardware emulators?	(4)	CO4
	OR		
4.d)	Explain how functional verification differs from structural verification.	(4)	CO4
Question No. 5			
5.a)	What are the limitations of true value simulation for large circuits?	(4)	CO5

OR

5.b)	What is concurrent fault simulation?	(4)	CO5
5.c)	How does testability affect fault coverage?	(4)	CO5

OR

5.d)	Describe one real-world application of statistical fault simulation.	(4)	CO5

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