



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:IV
Class:SY	Program:B.Tech
Branch Code:ETC	Pattern:2022
Name of Course:VLSI Design and Technology	Course Code:ETC222013
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Marks CO

Question No. 1

- 1a) Explain FPGA with neat architectural block diagram. (6) CO1

Question No. 2

- 2a) Write verilog code for full adder in structural modelling and behavioral modelling (6) CO2

Question No. 3

- 3a) Design and Implement 4:1 MUX using structural modelling (8) CO3

OR

- 3b) Explain four floors lift controller using verilog HDL code (8) CO3

- 3c) Write verilog code for full subtractor in dataflow modelling. Also show the boolean expression used. (8) CO3

OR

- 3d) Write verilog code for CMOS 3 input NOR gate in switch level modelling (8) CO3

Question No. 4

- 4a) Write short notes on : i) CMOS Inverter as not gate and ii) Noise margins in cmos inverter . (8) CO4

OR

- 4b) Design and implement 8:1 MUX using transmission gate (8) CO4

- 4c) Implement CMOS function $Y=ABC+D$ along with stick diagram (8) CO4

OR

- 4d) Implement $Y=[ABCD+EF]'$ using CMOS logic. Explain PDN & PUN for A=1,B=0, C=1, D=0, E=1, F=1 (8) CO4

Question No. 5

- 5a) What is the need of DFT. Explain in detail (8) CO5

OR

- 5b) Explain clock distribution technique (8) CO5
- 5c) Explain BIST with neat block diagram (8) CO5

OR

- 5d) For the given boolean function. extract the truth table with and without faults (S-A-0 at all inputs, S-A-1 at all inputs) $Y=AB+CD$ (8) CO5

..... End of question paper.....