



**K. K. Wagh Institute of Engineering Education & Research, Nashik**  
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:III
Class:SY	Program:B.Tech
Branch Code:ETC	Pattern:2023
Name of Course:Digital System Design with HDL	Course Code:2302203
Max. Marks:60	Duration:2.30 Hrs.

**Instructions:** Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

**Marks CO**

**Question No. 1**

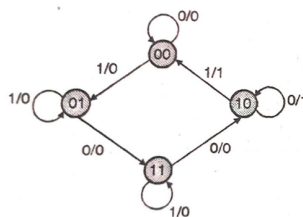
- 1a) Implement the function  $F(A,B,C,D) = \sum m(0,1,3,5,7,9,12,15)$  using 8:1 Mux by using folding technique (6) CO1

**Question No. 2**

- 2a) Design MOD 5 UP counter and explain with the help of waveforms (6) CO2

**Question No. 3**

- 3a) Design sequential circuit for the given state diagram using any Flip flop (8) CO3



**OR**

- 3b) Design mealy machine sequence detector for following sequence 101 using D flip flop (8) CO3

- 3c) Define ASM chart. State various types of boxes used for drawing the ASM chart. (8) CO3

**OR**

- 3d) Design a circuit which follows following sequence 2-3-4-5-6-7-2 (8) CO3

**Question No. 4**

- 4a) Compare TTL and CMOS logic families (8) CO4

**OR**

- 4b) What is architecture in VHDL explain with its syntax. Write VHDL code for Half adder (8) CO4

- 4c) With the help of example explain following statements in VHDL (8) CO4

1. If statement
2. Case statements

**OR**

4d) Draw and explain CMOS NOR gate. (8) CO4

**Question No. 5**

5a) Explain different modeling styles in VHDL. Explain different modeling styles in VHDL (8) CO5

**OR**

5b) Write VHDL code for 2 bit comparator (8) CO5

5c) Write VHDL code for full adder in behavioral modeling style (8) CO5

**OR**

5d) Write VHDL code for JK Flip flop (8) CO5

..... End of question paper.....