K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:III
Class:SY	Program:B.Tech
Branch Code:ELE	Pattern:2023
Name of Course:Analog and Digital Circuits	Course Code:2306206
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 02 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

		Marks	CO
Question No. 1			
1a)	Draw circuit diagram and derive the output of the differentiator Circuit using OPAMP.	(6)	CO2
Question No. 2			
2a)	Design a RC Phase shift Oscillator so that f_0=15 kHz. Assume suitable R1. C=0.01µF and Rf=29R1. Calculate R, Rf and draw circuit diagram.	(6)	CO4
Question No. 3			
3a)	In Binary weighted DAC, Find the output voltage when the input is 11011 (5 bit input), Assume Vr_{ef} =10 V , R_1= R_f=1 K Ω, also find resolution, full scale Voltage	(8)	CO4
	OR		
3b)	Design a sample-and-hold to hold Vin=3.00V for Thold=5 msec with maximum allowed droop Δ Vmax=2.0 mV Assume: • Net leakage current (switch + capacitor) Ileak=0.5nA • Use a unity-gain op-amp buffer (negligible input bias). Find: 1. Minimum hold capacitance Cmin. 2. Simple circuit sketch.	(8)	CO4
3c)	Draw and explain R-2R ladder Digital to Analog Converter.	(8)	CO2
	OR		
3d)	Draw and explain Dual Slope A to D converter.	(8)	CO2
Question No. 4			

4a)	Simplify the following expression using K-map f(A,B,C,D)= ∑ m(0,1,2,5,7,8,9,10,13,15)	(8)	CO3
	OR		
4b)	Minimize following Boolean expression using K-map and realize using logic gates. Y=A'B'C'D+A'BCD'+AB'C'D+ABC'D'	(8)	CO3
4c)	Design 4:2 priority encoder. Write truth table and draw logic diagram	(8)	CO3
	OR		
4d)	Design step by step a 3x 8 decoder. Write truth table, Draw circuit diagram	(8)	CO3
Question No. 5			
5a)	Design a synchronous counter that Counts the sequence 0, 1, 2, 4, 5, 6, 0. JK flip flop.	(8)	CO3
	OR		
5b)	What is Shift register? Explain the SISO and PISO mode	(8)	CO3
5c)	Explain the working principles, speed, power characteristics, and applications of SRAM and DRAM.	(8)	CO1
	OR		
5d)	Compare PAL, PLA, and FPGA in terms of structure, capability, and applications	(8)	CO1

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