



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:III
Class:SY	Program:B.Tech
Branch Code:INT	Pattern:2023
Name of Course:Digital Electronics & Logic Design	Course Code:2308206
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 2 page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Marks CO

Question No. 1

- 1a) Obtain the Sum of Products (SOP) and Product of Sums (POS) expression using K-map for - (6) CO1
 $Y = f(A,B,C,D) = \sum m (0,1,4,9,10,12,15) + d(3,11,13)$

Question No. 2

- 2a) Design a Full Subtractor using K-maps. (6) CO2

Question No. 3

- 3a) Explain the working of a 8:1 Multiplexer with a schematic diagram. (8) CO3
Implement $Y_1 = f(A,B,C,D) = \sum m (1,3,6,9,12,15)$ using 8:1 Multiplexer

OR

- 3b) Implement a Full Subtractor using an appropriate decoder and list the criteria used for selecting the suitable decoder for this implementation (8) CO3

- 3c) Implement the following Boolean Expressions (8) CO3

$$Y_1 = f(A,B,C,D) = \sum m (1,3,5,6,7,8,10) + d(2,12) \text{ and}$$

$$Y_2 = f(A,B,C,D) = \sum m (0,1,3,5,7,8,10,14) + d(2,11) \text{ using a Programmable Logic Array.}$$

OR

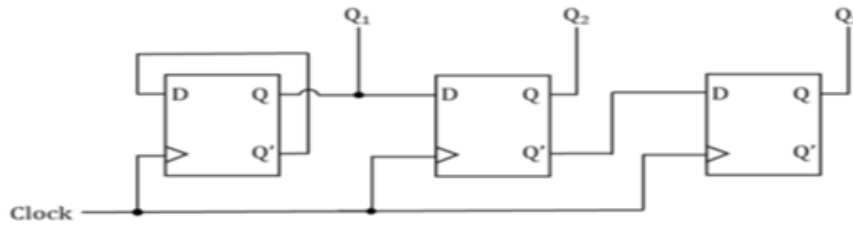
- 3d) Design and implement an odd parity checker for a 4 bit message. Explain how is odd parity bit obtained from a 4 bit message. (8) CO3

Question No. 4

- 4a) Obtain the Excitation table of T Flipflop and explain in detail. (5) CO4

OR

4b) Complete the timing diagram for the circuit, assuming all Q outputs begin in the high (logic 1) state. (5) CO4



4c) Explain the following for a D Flipflop- (5) CO4

- i) How to obtain D Flipflop from S-R Flipflop
- ii) Excitation table of D Flipflop
- iii) Any one Difference between D and T flipflop

OR

4d) Draw and explain the working of clocked S-R Flipflop. (using NAND/NOR Gates). Explain the Forbidden state. (5) CO4

4e) Draw and explain 3 bit universal shift register using D Flipflops (6) CO4

OR

4f) Draw and explain Johnson (Twisted Ring) Counter with initial state is $Q_3 Q_2 Q_1 Q_0 = "1110"$, from initial state explain all possible state (6) CO4

Question No. 5

5a) Design a 3 bit sequence detector to detect a sequence 101 arriving on an input X. Use T Flipflops. (8) CO5

OR

5b) Design a sequence generator to generate a binary sequence from 0100 to 1111 using IC 74191. (8) CO5

5c) Design a 4 bit synchronous DOWN Counter using T Flipflops. (8) CO5

OR

5d) Design a Synchronous Counter which will go through the states 3-0-7-2-5-3 using D Flip Flop. Avoid Lock out Condition. (8) CO5

..... End of question paper.....