K. K. Wagh Institute of Engineering Education & Research, Nashik

(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:IV
Class:SY	Program:B.Tech
Branch Code:INT	Pattern:2023
Name of Course:Computer Organization & Architecture	Course Code:2308216
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains ___2__page(s).
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

		Marks	CO
Question No. 1			
1a)	Explain Instruction Cycle in details	(6)	CO1
Question No. 2			
2a)	Explain how interrupt priority is handled in microprocessors.	(6)	CO2
Question No. 3			
3a)	Illustrate with a timing diagram how access time and cycle time affect read operations.	(5)	CO3
	OR		
3b)	Describe the various approaches to memory access in computer systems	(5)	CO3
3c)	Write the stepwise process of data flow from CPU to memory and back during read operations.	(5)	CO3
	OR		
3d)	What are the implications of locality on cache memory design?	(5)	CO3
3e)	Discuss the advantages and disadvantages of using Interrupt-driven I/O.	(6)	CO3
	OR		
3f)	Discuss how cache hit and miss rates affect CPU performance.	(6)	CO3
Question No. 4			
4a)	Differentiate between Maskable Interrupt (INTR) and Non-Maskable Interrupt (NMI) in 80386.	(5)	CO4
	OR		
4b)	Explain the following Flags of 80386 OF (Overflow Flag) DF (Direction flag) VM (Virtual Memory) flag	(5)	CO4

ZF (Zero Flag)

SF (Sign Flag)

4c)	Explain the register organization of 80386 microprocessor with a block diagram.	(5)	CO4

OR

4d)	Discuss how segmentation and paging work together for efficient memory management.	(5)	CO4
4e)	Explain following bits of Page Table Entry-	(6)	CO4

Page Frame Bits

Dirty bit

Accessed Bit

User/Supervisor Bit

Read/Write Bit

Present Bit

OR

4f)	Discuss the difference between privileged and non-privileged instructions with examples.	(6)	CO4

Question No. 5

5a)	Define Parallel Computing. Explain how it differs from serial computing.	(5)	CO5

OR

5b)	With suitable diagram, explain Distributed memory MIMD.	(5)	CO5
5c)	List and discuss the advantages and disadvantages of SIMD architecture.	(5)	CO5

OR

5d)	What are the challenges and disadvantages of using multicore architectures?	(5)	CO5
5e)	Explain how shared memory and cache are managed in SMP systems.	(6)	CO5

OR

5f)	Differentiate between SIMD, MIMD, and SISD systems based on Flynn's taxonomy.	(6)	CO5

····· End of question paper·····