



K. K. Wagh Institute of Engineering Education & Research, Nashik
(An Autonomous Institute From A.Y. 2022-23)

WINTER-2025	
Exam Seat No.:	
Academic Year:2025-2026	Semester:V
Class:TY	Program:B.Tech
Branch Code:ETC	Pattern:2023
Name of Course:Digital CMOS Design	Course Code:2302324
Max. Marks:60	Duration:2.30 Hrs.

Instructions: Candidates should read carefully the instructions printed on the Question Paper and on the cover page of the Answer Book, which is provided for their use.

1. This question paper contains 02 pages.
2. Answer to each new question is to be started on a new page.
3. Assume suitable data wherever required, but justify it.
4. Draw the neat labelled diagrams, wherever necessary.
5. The last columns indicates the Course Outcome and level of Blooms Taxonomy of the Question/sub-question.

Marks CO

Question No. 1

- 1a) Explain layout design rules. Draw the stick diagram and layout for a CMOS 2-input NAND gate. (6) CO1

Question No. 2

- 2a) With neat timing waveforms, explain low-to-high (TP_{LH}) and high-to-low (TP_{HL}) propagation delays. What are the parasitic capacitances in a MOSFET? (6) CO1

Question No. 3

- 3a) For a process technology with $L = 0.18 \mu\text{m}$, $n = 1.5$, $p = 3$, give the sizes of all transistors in a four-input NOR gate. (8) CO2

OR

- 3b) Write short notes on interconnect resistance and capacitance. Explain how they depend on physical parameters such as length, width, thickness, and spacing of interconnect. (8) CO2

- 3c) 2:1 Multiplexer using Transmission Gates (8) CO2

1. Derive the logic function for a 2:1 MUX.
2. Implement it using transmission gates and an inverter.
3. Explain the working principle for both selection states ($S = 0$ and $S = 1$).
4. Compare it with an implementation using CMOS logic.

OR

- 3d) Design a compound CMOS gate for the logic function (8) CO2

$$F = [(A+B)(C+D)]'$$

1. Draw the transistor-level schematic.
2. Draw CMOS layout using Euler's path.

Question No. 4

- 4a) Design a 3-to-8 Decoder using logic gates and explain the working principle. Write truth table and Boolean equations. Draw the logic diagram. (8) CO2

OR

- 4b) Explain the concept of metastability in flip-flops. Derive the expression for Mean Time Between Failures (MTBF) and explain methods to improve MTBF. (8) CO2
- 4c) For a given boolean function $F(A,B,C)=A'B'+BC$. Find possible static-1 hazards and remove them by factoring or adding consensus(redundant) if safe. (8) CO2

OR

- 4d) Write the Verilog HDL code for a 4-bit Parallel Adder. Also explain the test bench. (8) CO2

Question No. 5

- 5a) Explain the concept of domino logic and why it is used in high-speed circuits. Draw the domino implementation of a 3-input AND gate. Discuss the limitations and precautions while using domino logic. (8) CO3

OR

- 5b) Write short notes on: NORA logic & BiCMOS circuits (8) CO3
- 5c) Compare static CMOS logic with Dynamic logic circuits, highlighting the advantages and disadvantages of static CMOS in terms of: Noise immunity, Power consumption, Speed, Design complexity. (8) CO3

OR

- 5d) What is a dynamic CMOS circuit? Explain cascading & charge sharing problems in dynamic logic. (8) CO3

..... End of question paper.....