May 2017

Total No. of Questions—8] [Total No. of Printed Pages—3

Seat No.	

[5152]-564

S.E. (Computer) (I Sem.) EXAMINATION, 2017

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of calculator is allowed.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Multiply the following using Booth' algorithm [6]

Multiplicand = +11

Multiplier = –6.

(*b*) Explain in brief seven RAID levels. [6]

Or

2. (*a*) Show the general structure of IAS Computer and explain. [6]

(*b*) Draw and explain the flowchart of restoring division algorithm. [6]

P.T.O.

3. (*a*) What is the use of DMA ? Explain cycle stealing in DMA. [6]

(*b*) Explain the following addressing modes with one example each : [6]

(*i*) Immediate

(*ii*) Register Indirect

(*iii*) Direct Addressing

Or

4. (*a*) Differentiate between programmed I/O and interrupt driven I/O. [6]

(*b*) What is machine instruction ? Explain types of instructions. [6]

5. (*a*) What are various hazards in instruction pipelining ? Explain. [7]

(*b*) Write a short note on superscalar execution and superscalar implementation. [6]

Or

6. (*a*) Explain the instruction cycle in detail. [6]

(*b*) List and explain various ways in which an instruction pipeline can deal with conditional branch instructions. [7]

7. (*a*) Compare horizontal and vertical microinstruction format. [6]

(*b*) Explain in detail microinstruction sequencing organization. [7]

Or

8. (*a*) Compare Hardwired control over micro-programmed control. [6]

(*b*) Write a control sequence for the following instruction for single bus organization : ADD (R3), R1. [7]