

Nov-2017

Total No. of Questions—8]

[Total No. of Printed Pages—3

Seat No.	
----------	--

[5252]-569

S.E. (Computer) (Second Semester) EXAMINATION, 2017

MICROPROCESSOR

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Solve Q. 1 or Q. 2; Q. 3 or Q. 4; Q. 5 or Q. 6;

Q. 7 or Q. 8.

- (ii) Neat diagrams must be drawn wherever necessary.
- (iii) Figures to the right indicate full marks.
- (iv) Assume suitable data, if necessary.

1. (a) Explain immediate and register addressing mode with an examples. [2]

(b) Explain with example SHL and ROL instructions. [4]

(c) Explain in detail the control registers of 80386. [6]

Or

2. (a) Explain MSW. [2]

(b) Explain paging mechanism. [4]

(c) Explain the following instructions, mention flags affected : [6]

(i) LIDT

(ii) CLD

(iii) MOVS.

3. (a) What is CPL and RPL ? [2]

(b) Differentiate between memory mapped I/O and I/O mapped I/O. [4]

(c) Draw and briefly explain Task State Segment. [6]

Or

4. (a) When does a page fault occur ? [2]

(b) Explain any two I/O privilege instructions. [4]

(c) Explain what happens when an interrupt calls a procedure as an interrupt handler. [6]

5. (a) What are the contents of various registers of processor 80386 after reset ? [3]

(b) How many debug registers are present in 80386 ? List and draw all of them. [4]

(c) With neat diagram explain the process of linear address formation in V86 mode. [6]

Or

6. (a) Write short note on "Instruction Address Breakpoint". [3]

(b) What all initializations required to start processor in real mode after reset ? [4]

(c) With neat diagram explain "Entering and leaving V86 mode". [6]

P.T.O.

[5252]-569

2

7. (a) Explain HOLD and HLDA signals of 80386DX. [3]
(b) List various bus states when address pipelining is used. [4]
(c) Draw read cycle with non-pipelined address timing. [6]

Or

8. (a) Explain the following signals : [3]
(i) NMI
(ii) INTR
(iii) RESET
(b) Draw and explain 80387 register stack. [4]
(c) Draw 'write cycle with pipelined address timing'. [6]