Total No. of Questions : 10]

SEAT No. :

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[5153]-590

T. E. (Computer Engineering)

DIGITAL SIGNAL PROCESSING APPLICATIONS

(2012 Course) (Semester-II) (End Sem.) (310253)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) *Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.*
2) *Neat diagram must be drawn wherever necessary.*
3) *Assume suitable data, if necessary.*

Q1) a) State the sampling theorem and explain in brief the coding process of ADC. [5]

b) Obtain the Z Transform(ZT) of a DT signal

$x(n) = a^n u(-n-1)$ Sketch the ROC. [5]

OR

Q2) a) A CT signal having frequency 50 Hz is sampled at a rate of 1200 samples /sec. Obtain

i) Number of samples per cycle.
ii) Digital/Discrete frequency f and ω.
iii) Minimum sampling rate to avoid aliasing effect.
iv) Period of a DT signal. [5]

b) State and prove the time shifting property of Fourier Transform(FT). Define it for DFT. [5]

Q3) a) Compare Linear Convolution with Circular Convolution. [5]

b) Define N point DFT by means of twiddle factor and obtain the twiddle factors for 4 point DFT. [5]

OR

Q4) a) Obtain the computational complexity of Radix-2 DIF FFT Algorithm. [5]

b) Define the system, function and obtain it for the given system described as- $y(n)-\frac{5}{6}y(n-1)+\frac{1}{6}y(n-2)=x(n)-\frac{1}{2}x(n-1)$ [5]

P.T.O.

Q5) a) Derive the Direct Form-II IIR filter structure from the system function H(Z) and realize it using multipliers, adders and delay elements. [9]

b) Obtain and realize linear phase FIR filter structure having impulse response

$$h(n)=\delta(n)+\frac{1}{2}\delta(n-1)-\frac{1}{4}\delta(n-2)+\frac{1}{2}\delta(n-3)+\delta(n-4)$$ [9]

OR

Q6) a) Obtain and draw the cascade form realization for IIR filter having transfer function $H(Z)=\frac{5Z(Z+0.4)}{(Z-0.2)(Z-0.6)}$ [9]

b) Represent the mathematical form of Nth order FIR filter by means of system function H(Z). Draw the Direct Form filter structure and determine the number of multipliers, adders and delay elements required to realize the filter. [9]

Q7) a) Compare conventional Microprocessor with DSP Processor architecture. Draw and expain basic building blocks of DSP processor. [8]

b) Drarw and explain the SIMD(Single Instruction Multiple Data) architecture of SHARC DSP processor. [8]

OR

Q8) a) Explain the features of SHARC DSP processor. List the number of DAGs with its capabilities and memory pointer registers supported by DAG. [8]

b) What is OMAP? Explain the features and applications of OMAP in brief. [8]

Q9) a) What is Companding? What is its significance in audio processing? What is the impact of data rate on sound quality? [8]

b) With mathamatical form, explain any two gray level transforms used for image enhancement. [8]

OR

*Q10)*a) Draw and explain Human Speech Model in speech synthesis and recognition. [8]

b) How digital image is represented by means of digital computer? How gray scale image is different than colour image? What is Histogram of an image? [8]

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