[4959] - 1163

B.E. (Computer Engineering)
High Performance Computing
(2012 Pattern)

Time : 2½ Hours]

Instructions to the candidates:

[Max. Marks : 70

1) First Two Questions are Compulsory. Answer three questions. (Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.)
2) Neat diagrams must be drawn wherever necessary.
3) Assume suitable data if necessary.

Q1) a) Explain SIMD, MIMD and SIMT architecture. **[4]**

b) Explain basic working principal of VLIW processor. **[6]**

Q2) a) Write a note on IBM Cell Broadband Engine (CBE). **[6]**

b) Write a short note on Dataflow Model. **[4]**

Q3) a) Differentiate between Thread and Process. For Multi threading implementation there is implicit support of architecture. Justify. **[7]**

b) Explain how 'pthread_mutex_trylock' reduce locking overhead? **[8]**

OR

Q4) a) Implement Producer Consumer problem using Mutex synchronization primitives in Pthreads. **[7]**

b) Describe Barrier Synchronization for Shared address space Model. **[8]**

P.T.O.

a) Write a pseudo-code for Parallel Quick Sort.

b) How pivot selection is crucial factor for algorithm performance? [7]

[8]

OR

a) Explain sorting network with suitable diagram.

b) Explain single source shortest path algorithm with suitable example. [7]

[8]

a) Write a short note on (Any Two):

   i)   Discrete optimization problems. [15]

   ii) Parallel Best-First-Search.

   iii) Quantum Computers.

b) Share your thoughts about how HPC will help to promote "MAKE IN INDIA" initiative.

[5]

OR

a) Write a short note on (Any Two): [15]

   i)   Parallel Depth-First-Search.

   ii) Search Overhead Factor.

   iii) Power Aware Processing.

b) Define term HPC and Elaborate its use to Indian Society. [5]

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